

1	Cover Page
2	Block Diagram
3	Clock Generator
4	Power (CPU Vcore)Intersil 6566(DCR Sense)
5	Power A(DC to DC)
6	Power B(DC to DC),PWR sequence&good
7	K8 - M2 CPU (HT) D
8	K8 - M2 CPU (MEM) A
9	K8 - M2 CPU (CTRL) B,C
10	K8 - M2 CPU (POWER,GND) E,F,G,H
11	DIMM1 & DIMM2(Dual Channel)
12	DIMM3 & DIMM4(Dual Channel)
13	DDR2 DIMMS POWER
14	DDR2 TERMINATION
15	NB - RS485/AMD690G(HT LINK0 IF) A
16	NB - RS485/AMD690G (PCI-E LINK I/F) B
17	NB - RS485/AMD690G (SYSTEM I/F) C
18	NB - RS485/AMD690G (POWER & GND) D,E
19	PCI Express Slot x16 & x1
20	SB - ATI SB600(PCIE, PCI, CPU, LPC)
21	SB - ATI SB600(APIC, GPIO, AUDIO, USB)
22	SB - ATI SB600(SATA, IDE,HWM,SPI)
23	SB - ATI SB600(STRAPS, PWR, DECOUPLING)
24	LPC SIO-ITE8716F/IX, LPC ROM
25	PCI 1, PCI2
26	PCI Extender & VGA & DVI
27	USB, IDE
28	COM, LPT
29	Front Panel, FAN
30	LAN (RTL8100SB/8100C)
31	AUDIO ALC888/883/660 (CHIP)
32	AUDIO ALC888/883/660 (PANEL)
33	POWER DELIVERY CHART
34	CLOCK DISTRIBUTION

# AMD690GM-M2

BASED ON RES485-M VER:A  
PCB: 244mm\*244mm

Rev : 1.0A L2:PWR  
L3:GND

## Rev.B

- 1.Remove AC97\_OSCIN connection(R610, C550) (PAGE 3)
- 2.R270 change to 56K, R247 change to 100K (PAGE 4)
- 3.Remove pull up resistor R328, R329 (PAGE 6)
- 4.Add R668 to connect VCC1.2 and VCC1.2\_SB (PAGE 6)
- 5.Add Q41, R271, R272 to level shift (PAGE 7)
- 6.Remove SID connection (R655) and pull up resistor (R225) (PAGE 7)
- 7.SC38, SC54, C256, C257, C232, C250 change to 180P (PAGE 10)
- 8.Add pull up resistor R450 (PAGE 20)
- 9.Remove -REQ2, -REQ4, -GNT2, -GNT4, -LPC\_DRQ1 (PAGE 20)
- 10.VCC1.2 change to VCC1.2\_SB (PAGE 20)
- 11.Remove WD\_PWRGD connection (R596) (PAGE 21)
- 12.Remove FB61, FB62 (PAGE 22)
- 13.VCC1.2 change to VCC1.2\_SB (PAGE 22)
- 14.Remove R473, R436 (PAGE 23)
- 15.VCC1.2 change to VCC1.2\_SB (PAGE 22)
- 16.R457 connect VCC1.2 change to connect VCC1.8 (PAGE 23)
- 17.ROM1 pin7 connect to -WP\_ROM1 (PAGE 24)
- 18.C457 change to 10U (PAGE 24)
- 19.Add C155, C156 for EMI (PAGE 25)
- 20.SRN1, SRN2 change to SL1, SL2, SL3, SL4 (PAGE 26)
- 21.U27 pin28 connect to JLEPC1 pin18 (PAGE 26)
- 22.Remove C6, C7, C8, C9 (PAGE 26)
- 23.Remove 3pin smart fan (PAGE 29)
- 24.USBLAN1 change to Speed Tech P25@153-P5P9 (PAGE 30)
- 25.C66 change to 0.1U (PAGE 30)
- 26.Add C5, C44, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76 for EMI (PAGE 32)

## Rev.1.0

- 1.REMOVE ALC655 CO LAY

## DETECT PIN

IR	SIO:GP23(PIN24)
COM2	SIO:GP25(PIN22)
AC'97	SIO:GP26(PIN21)
WOL	SIO:GP31(PIN18)
S3	SIO:GP32(PIN17)
CNR	SIO:GP33(PIN16)
TVOUT	SIO:GP34(PIN14)
5.1/7.1	SIO:GP35(PIN13)
RESERVED	SIO:GP37(PIN11)

## IDE Cable detect

-P66DET	SB: GPIO9
---------	-----------

## LED Blinking

G_LED1	SIO:GP10(PIN84)
G_LED2	SIO:GP53(PIN77)

## Other

BIOS_WP	SIO:GP41(PIN28)
WT_BEEP	SIO:GP16(PIN29)
SIO_S4S5	SIO:GP40(PIN79)
GPO_LAN	SIO:GP30

## Voltage Adjustment

VCC18	SIO_GPO20
	SIO_GPO21

## PCI Bus Resource

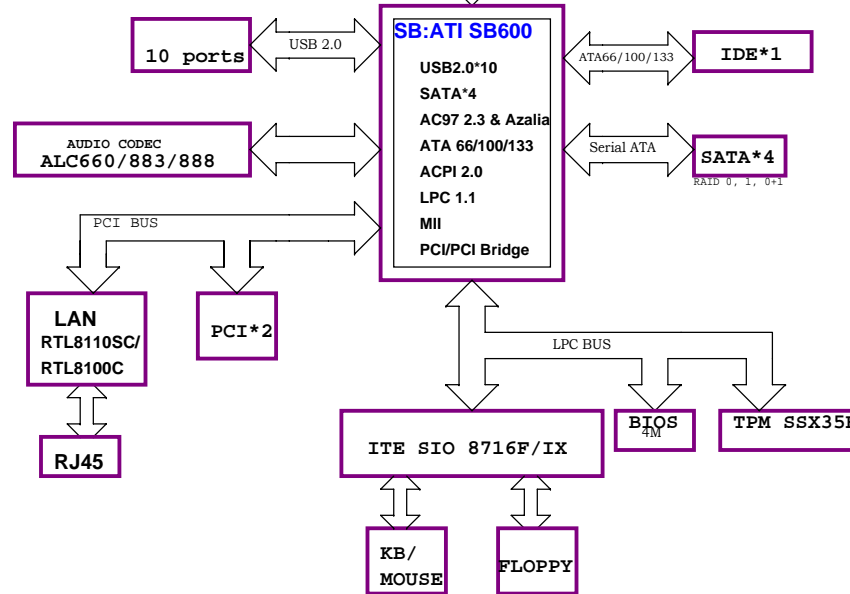
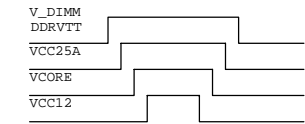
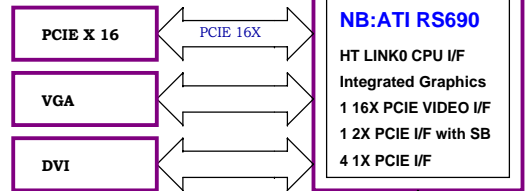
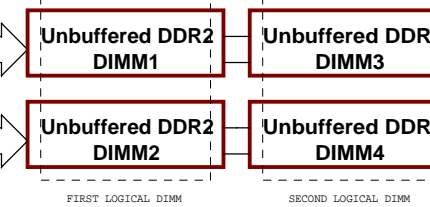
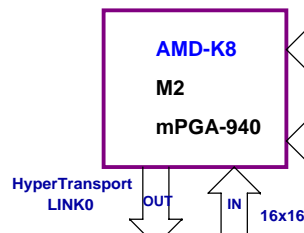
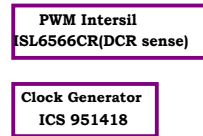
PCI1	AD16	INT E, FGH	REQ0
PCI2	AD17	INT F, GHE	REQ1
LAN	AD21	INT G	REQ3



Elitegroup Computer Systems

Title			
Cover Page			
Size	Document Number		Rev
Custom	AMD690GM-M2		1.0A
Date:	Monday, December 18, 2006		Sheet 1 of 34

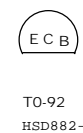
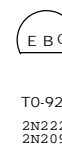
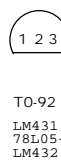
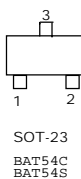
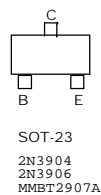
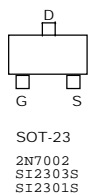
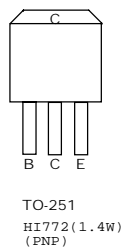
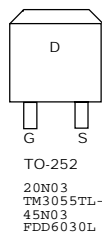
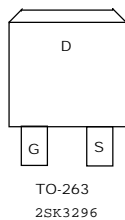
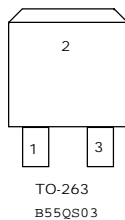
High Side\*2 TO-252  
Low Side\*2 TO-252



#### Layout width/space

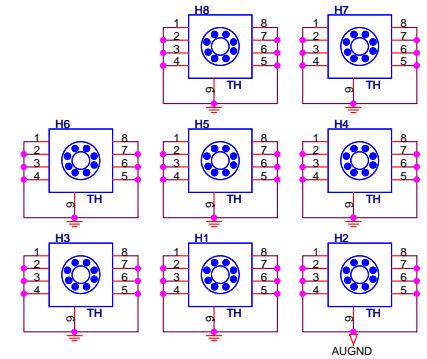
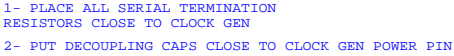
	PCB 2116	
USB(45/90)	20/8/8/8/20 20/8/8/8/20	(47/87) layout(47/87)
LAN(50/100)	20/8/12/8/20 20/8/10/8/20	(47/91) layout(47/90)
SATA(50/100)	20/6/6/6/20 20/5/7/5/20	(57/98) layout(62/111)
PCI-E(50/100)	20/6/6/6/20 20/5/7/5/20	(57/98) layout(62/111)
1394(55/110)	20/6/9/6/20 20/6/9/6/20	(56/105) layout(56/105)
R.G.B (37.5)	20/9/18/9/18/9/20 25/5/25/5/25/5/25	ATI DEMO Put 75 ohm on NB (Impedance=37.5 ohm)

22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



www.schematic-x.blogspot.com

Elitegroup Computer Systems		
Title		
Block Diagram		
Size	Document Number	Rev
Custom	AMD690GM-M2	1.0A
Date:	Monday, December 18, 2006	Sheet 2 of 34

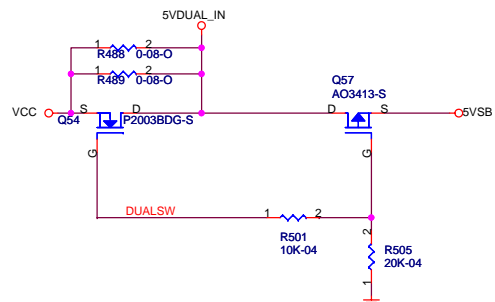
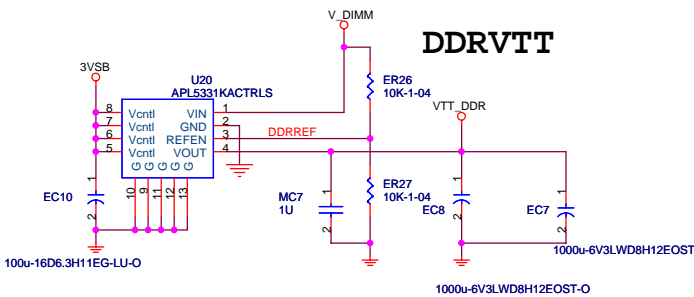
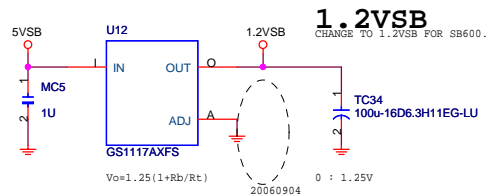
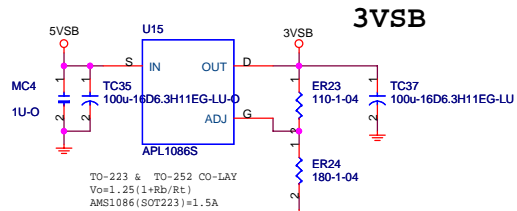


FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

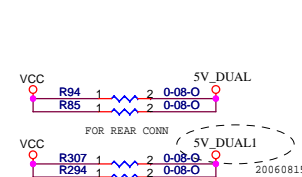
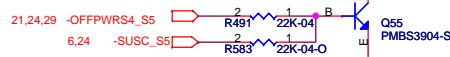
```
FS0,1,2 internal pull low(120K ohm)
```



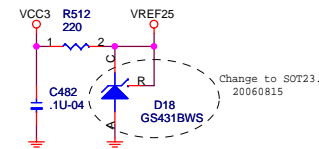
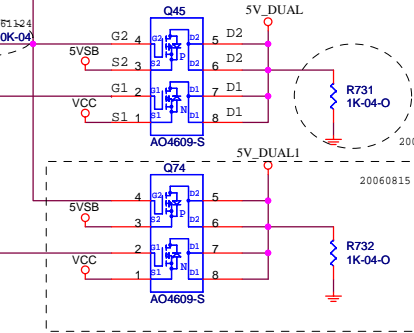
Status	Target	Super I/O F/GXS
AC plug	5V_DUAL=0	SIO_S4S5=0,D=1
S0,S1	5V_DUAL=VCC	SIO_S4S5=1
S3	5V_DUAL=5VSB	SIO_S4S5=0
S4,S5	5V_DUAL=5VSB	SIO_S4S5=0
S4,S5	5V_DUAL=0	SIO_S4S5=1



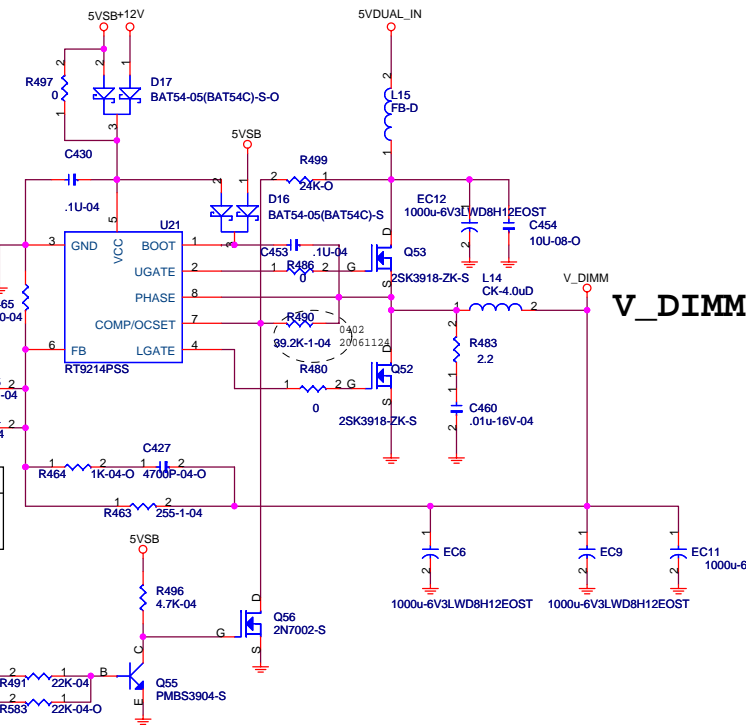
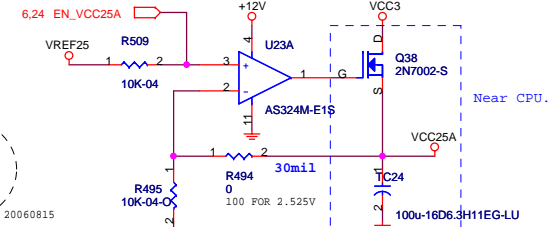
SIO_GP20	SIO_GP21	V_DIMM
1	1	Normal
0	1	+50mV
1	0	+100mV
0	0	+150mV



## 5V\_DUAL

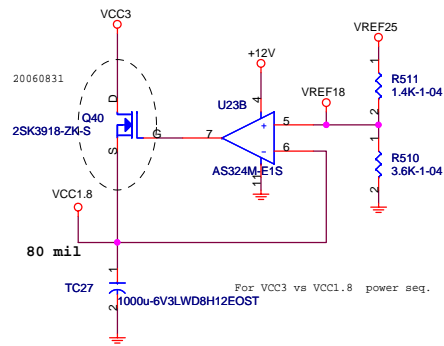


## VCC25A

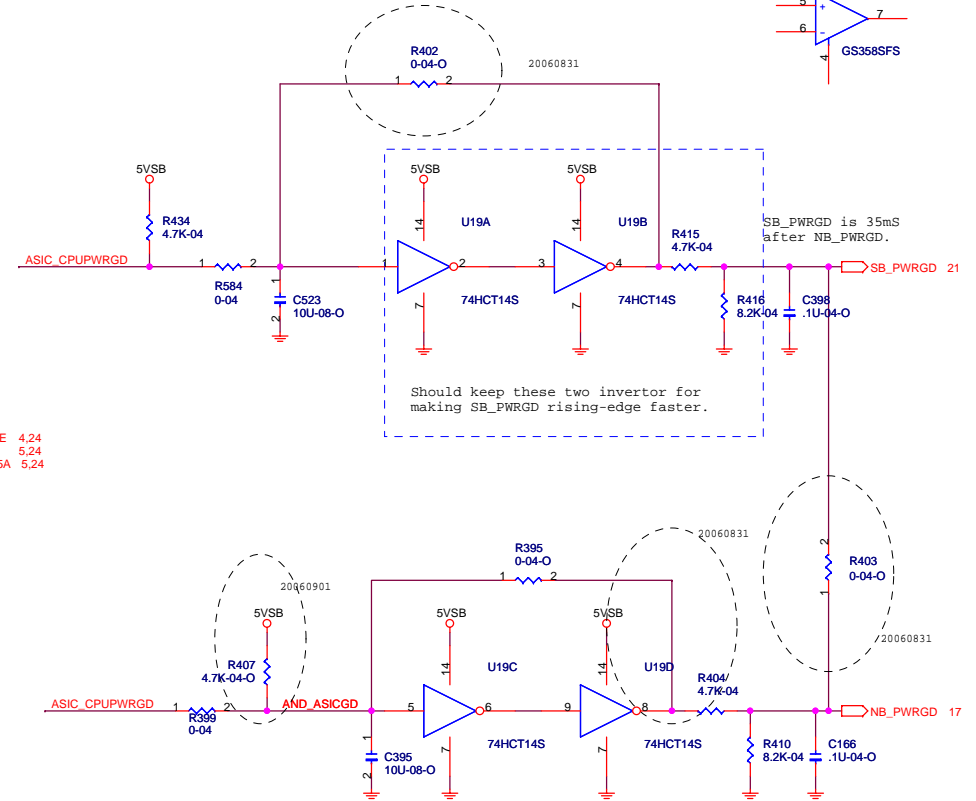
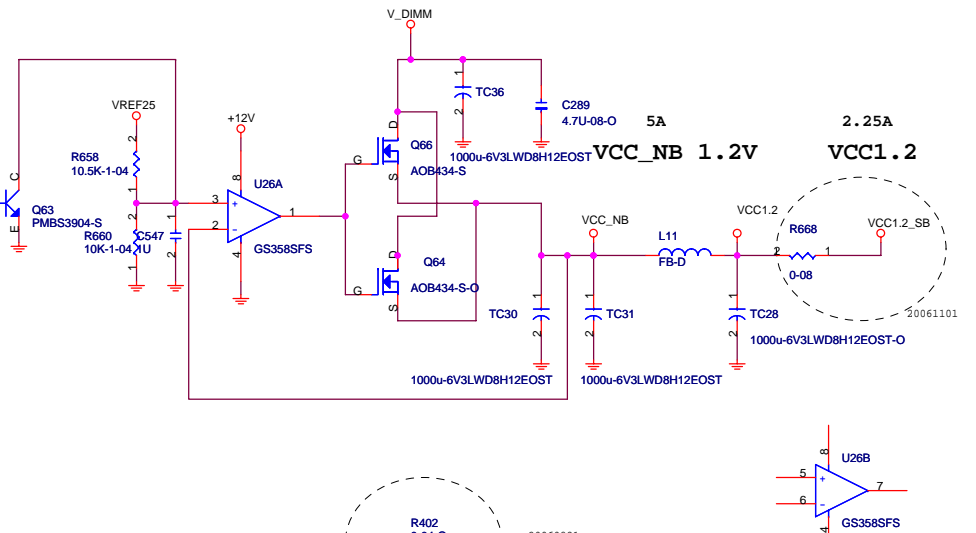
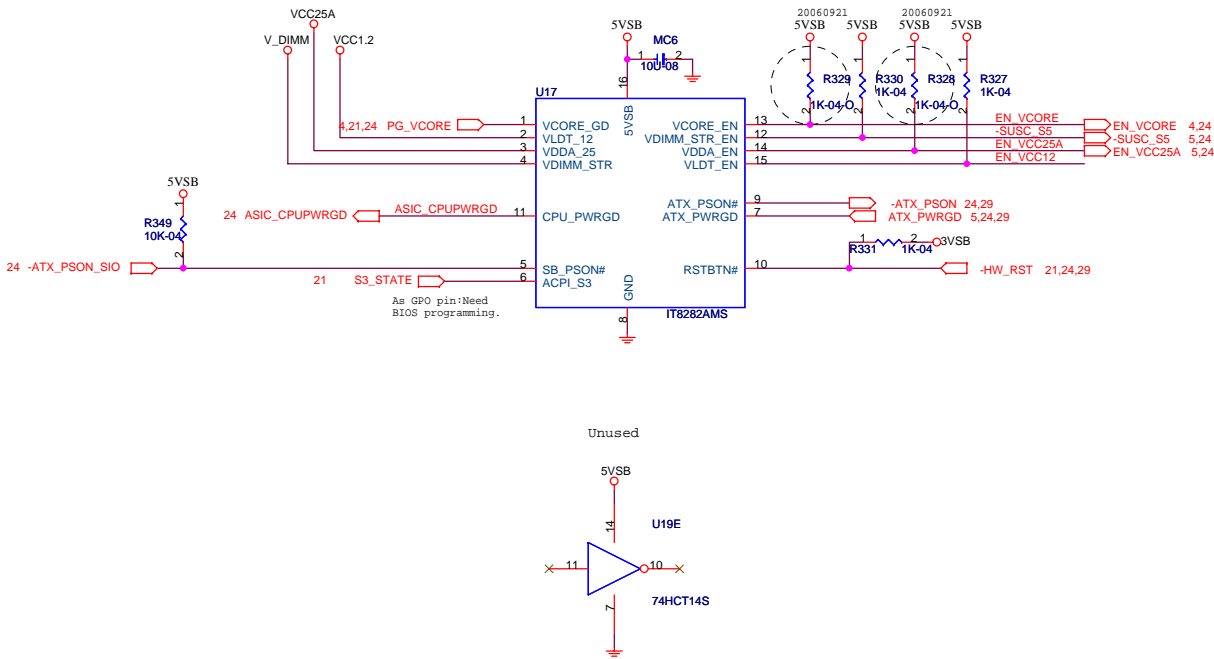


## V\_DIMM

## VCC1.8

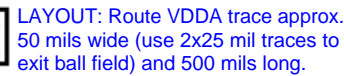


## K8 Power Sequence



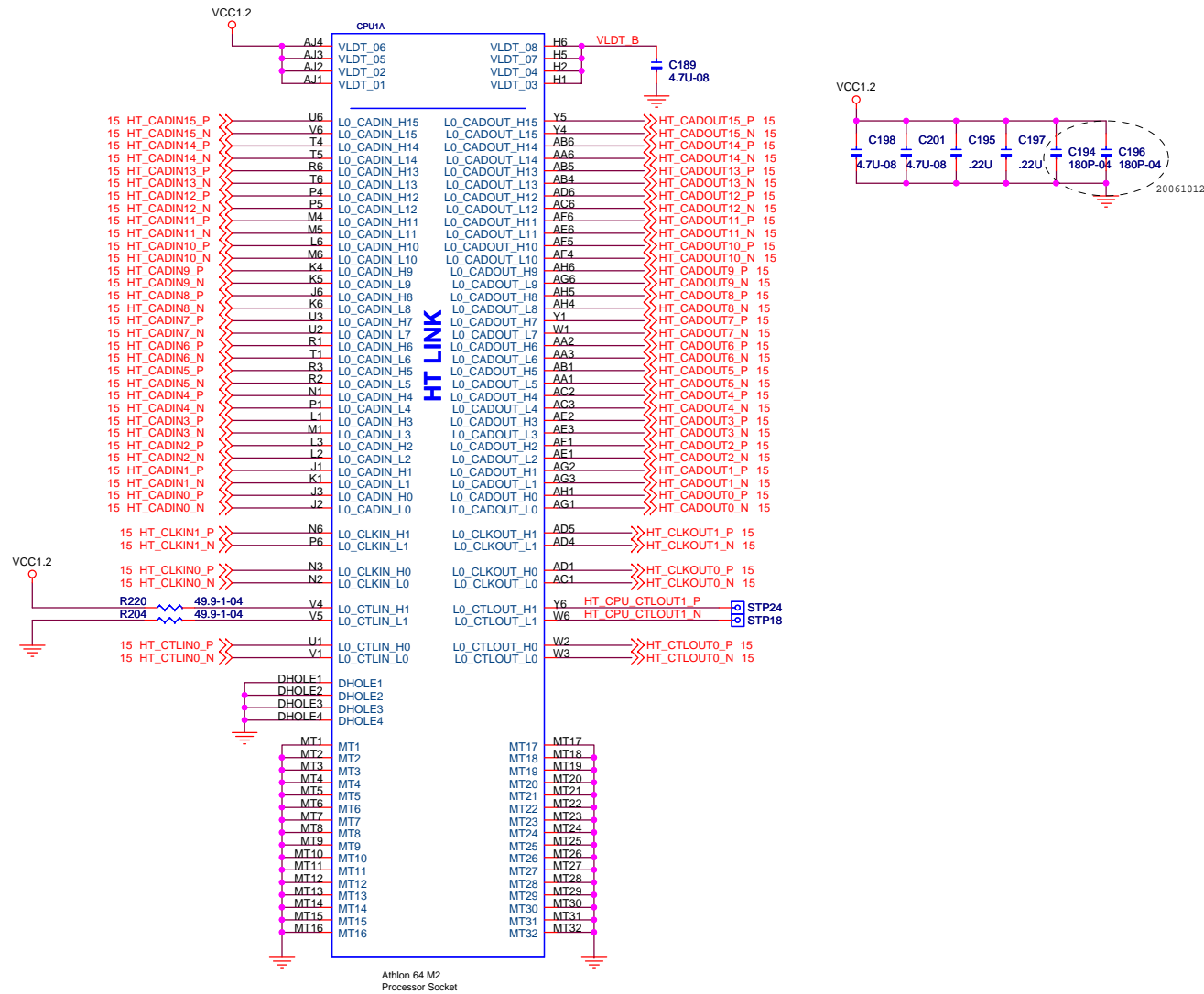
Required for compatibility  
with future processors

20060803



## CPU HyperTransport Interface

VDDLDRUNCPU is connected to the VDD\_LDT\_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



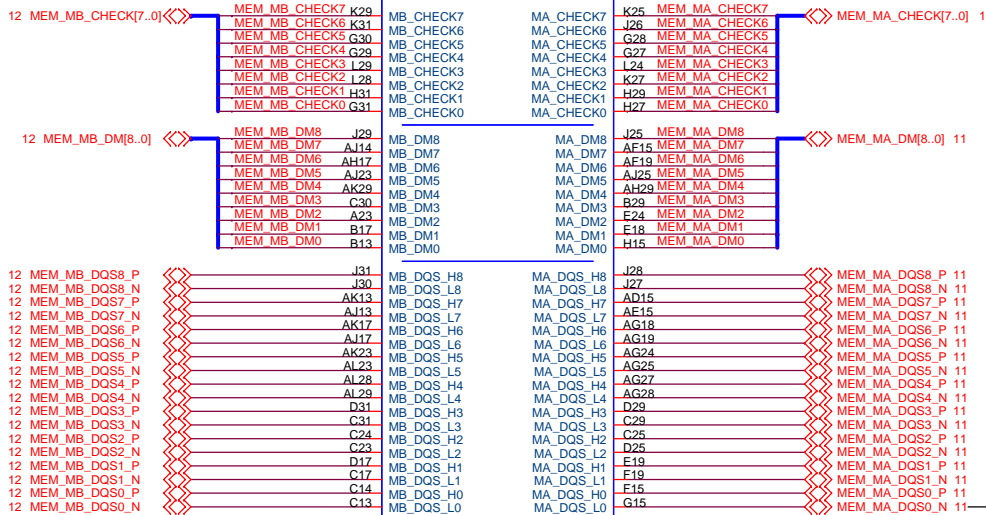


# Processor DDR2 Memory Interface



VDD\_VTT\_SUS\_CPU is connected to the VDD\_VTT\_SUS power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

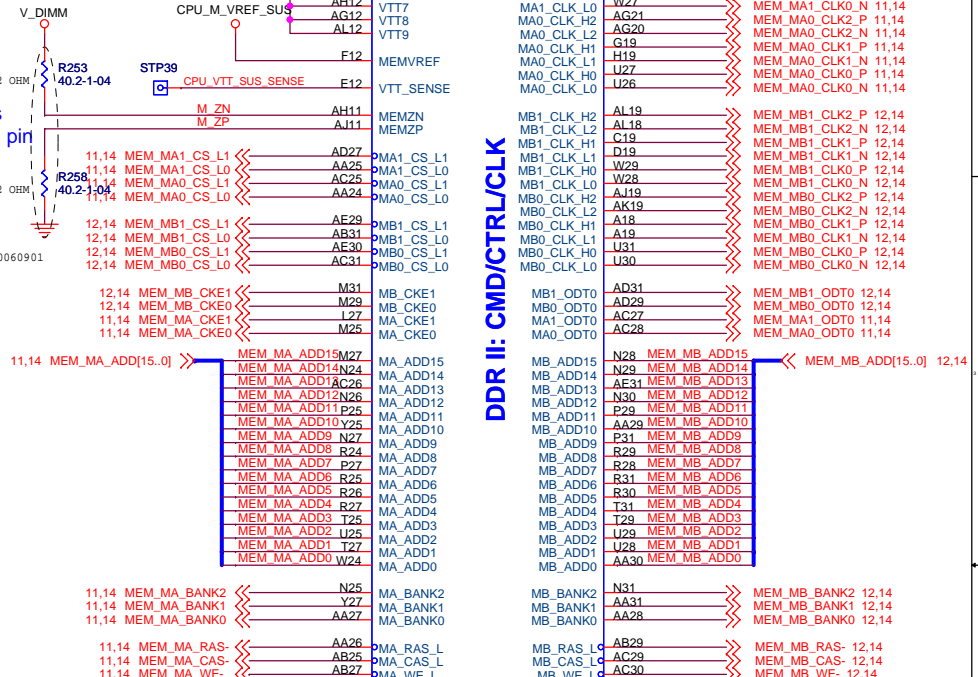
To upper DIMM sockets for each  
Logical DIMM (DIMM2 and DIMM4).



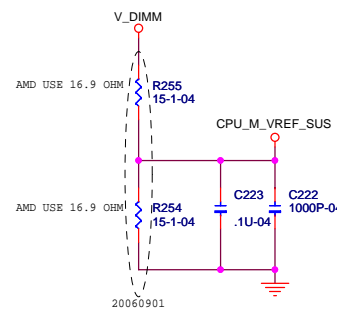
Athlon 64 M2  
Processor Socket

Keep trace to resistors  
less than 1" from CPU pin

To lower DIMM sockets for each  
Logical DIMM (DIMM1 and DIMM3).



## VDD\_VREF\_SUS\_CPU



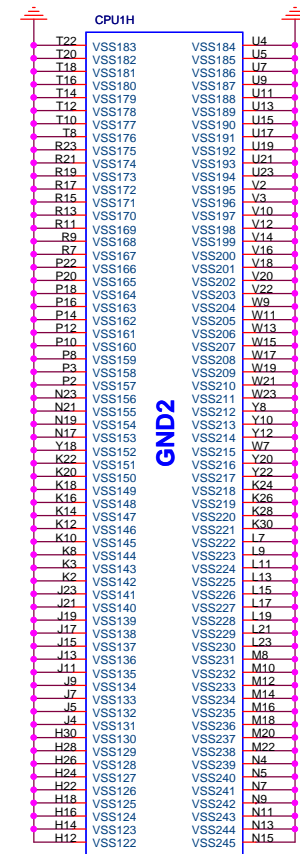
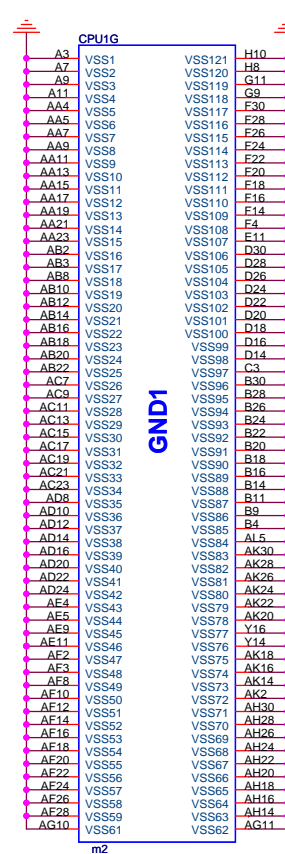
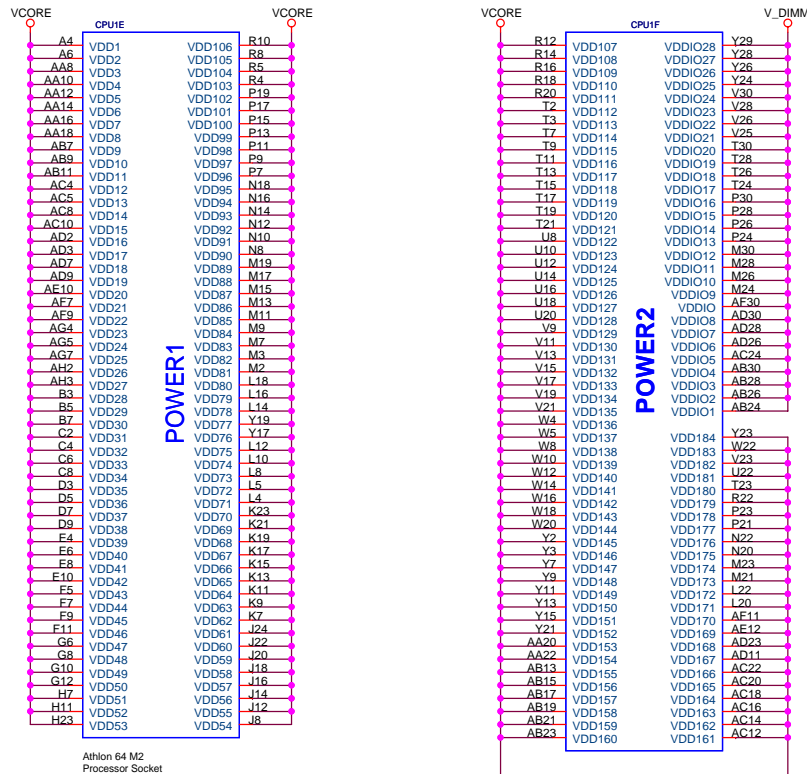
**Elitegroup Computer System**

File: **M2 DDR2 MEMORY I/F**

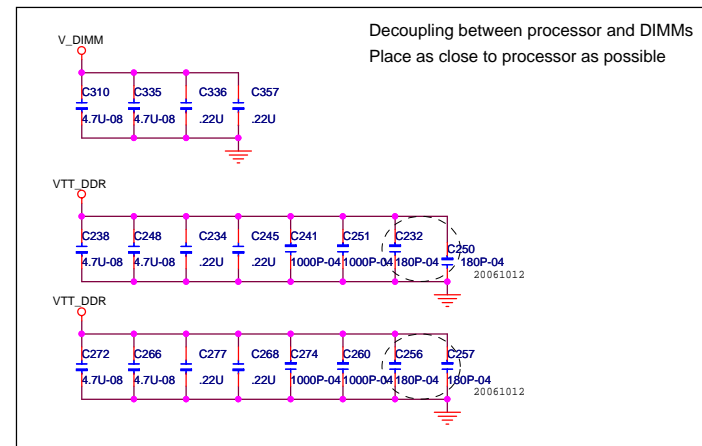
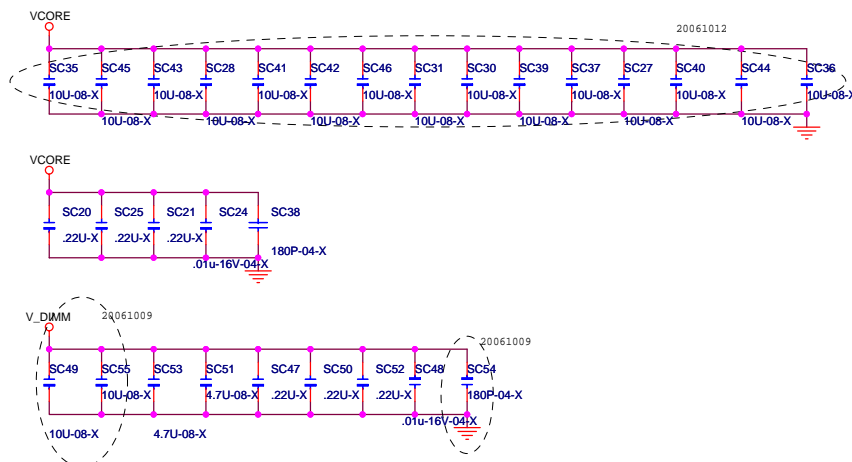
Size C Document Number **AMD690GM-M2** Rev **1.0A**

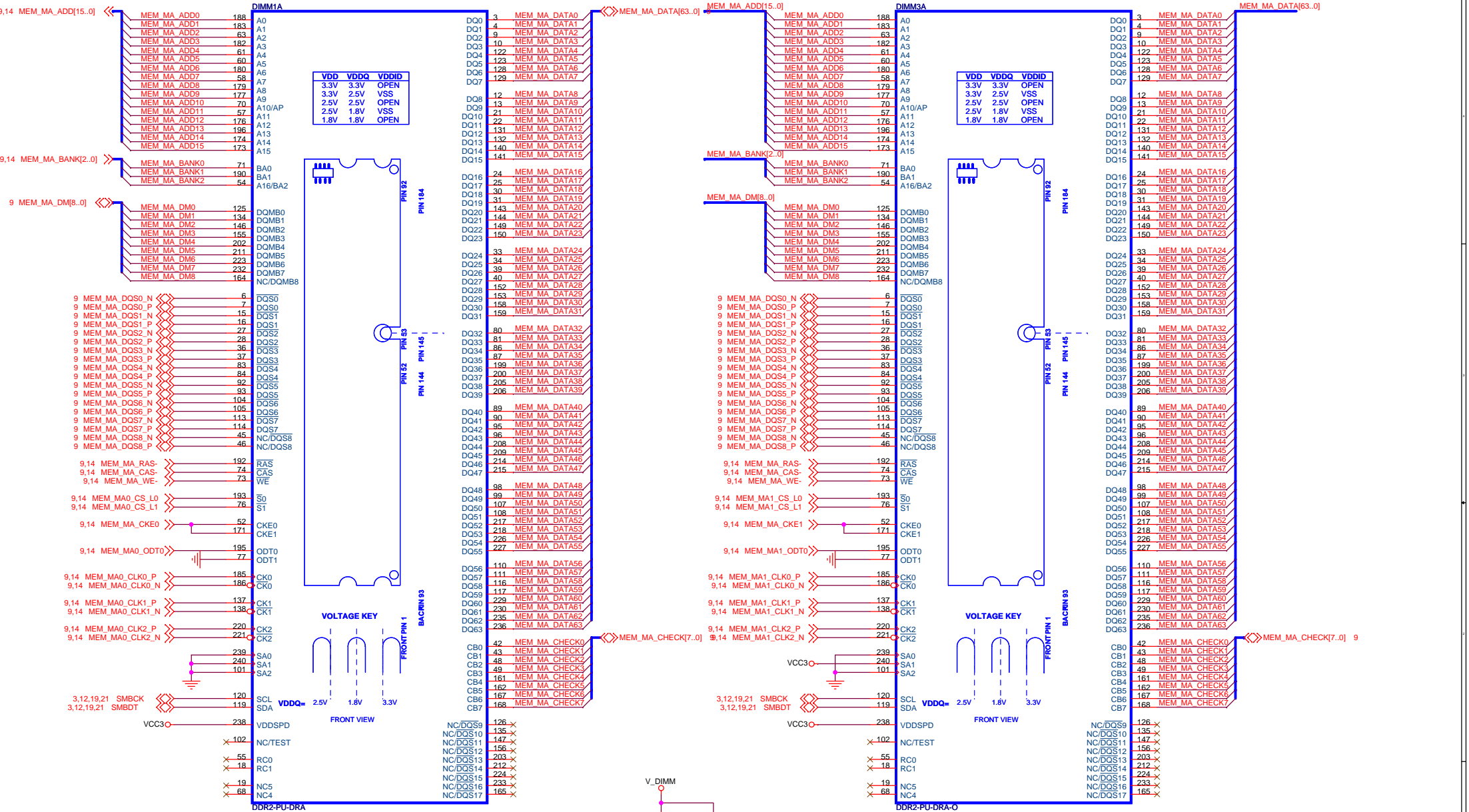
Date: Tuesday, December 19, 2006 Sheet 9 of 34

# Processor Power and Ground



## Bottomside Decoupling

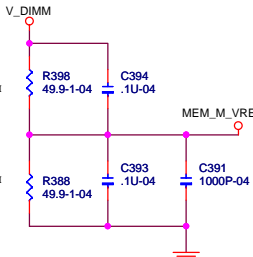


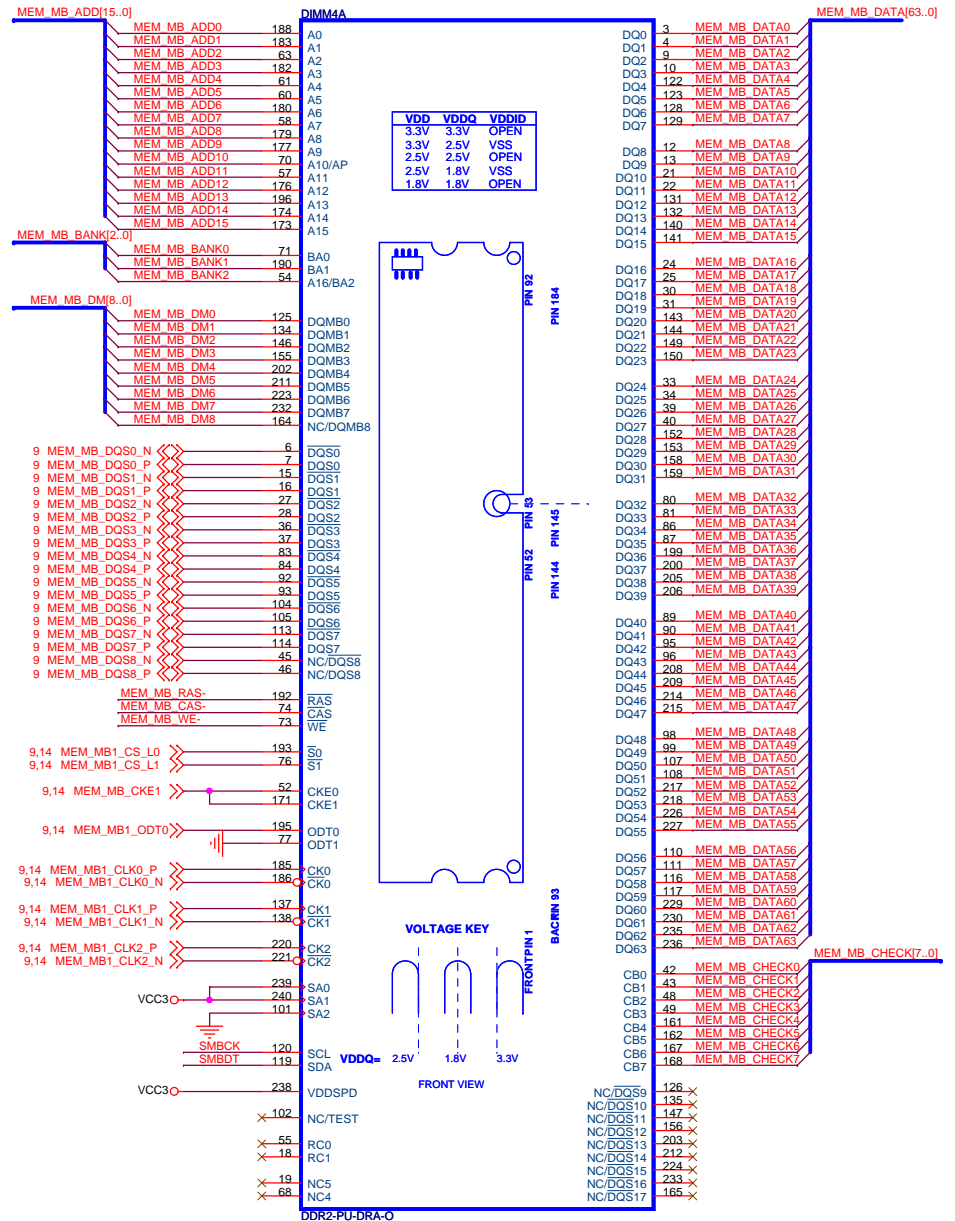
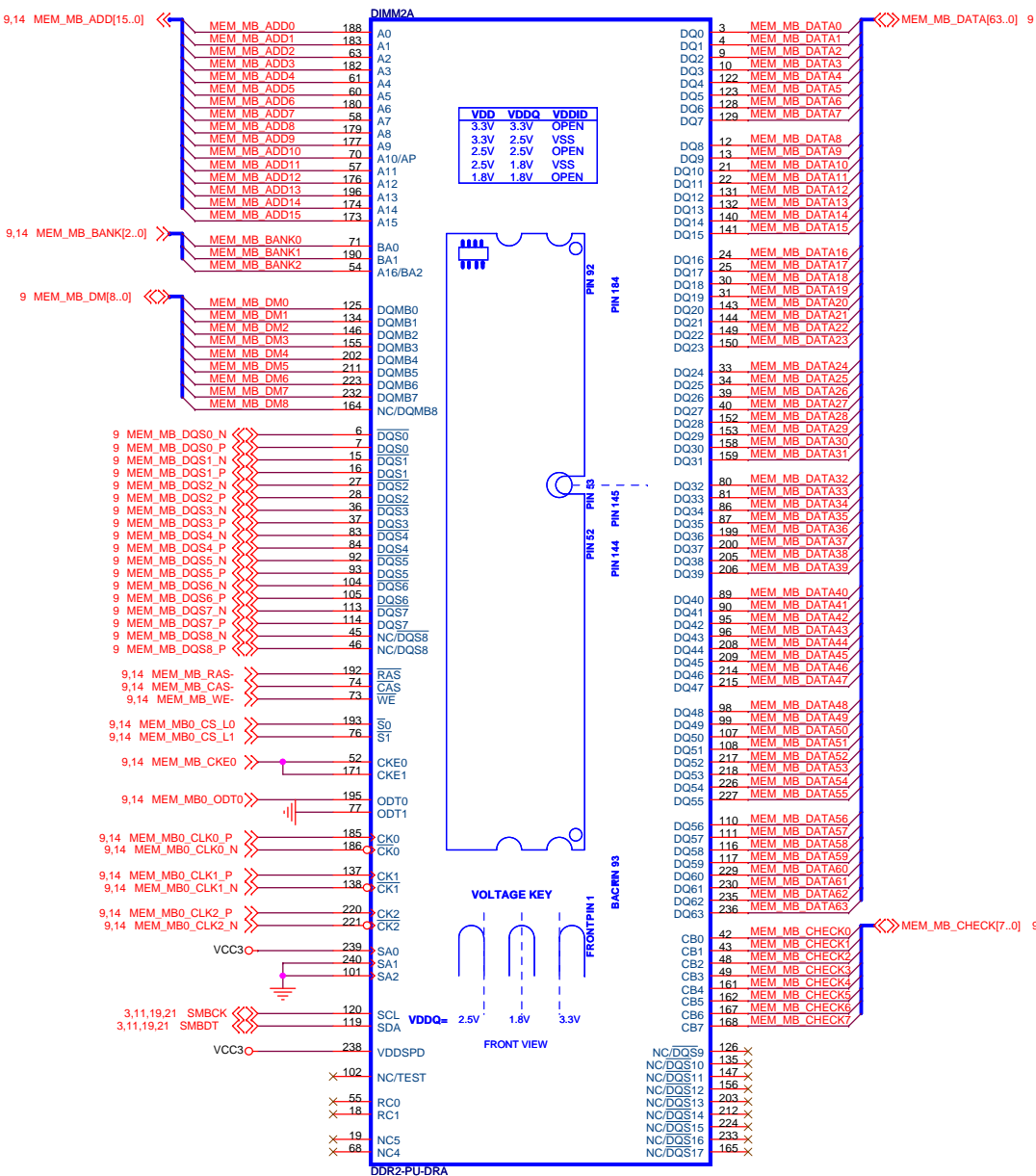


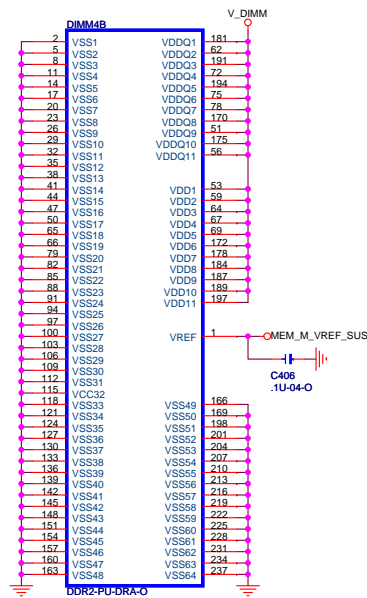
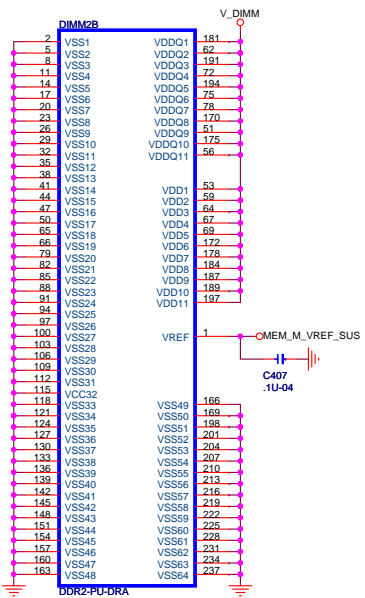
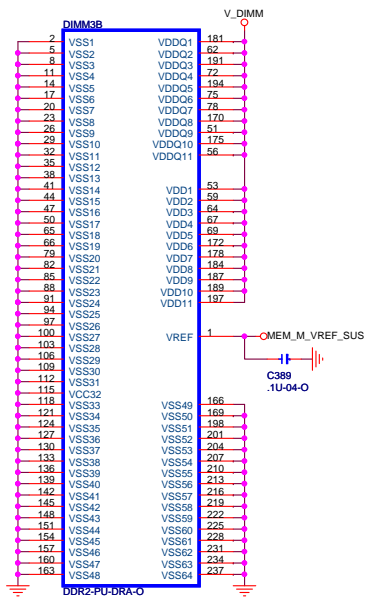
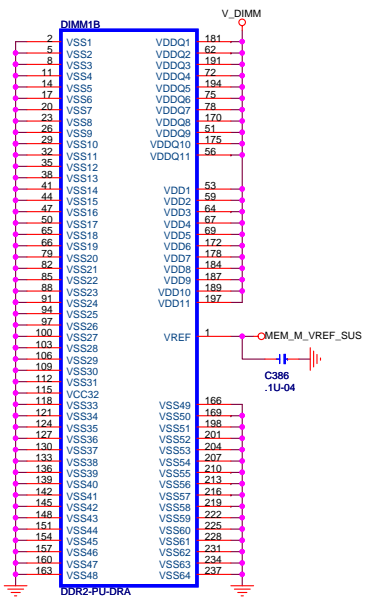
VDD\_VREF\_SUS\_MEM

AMD USE 59 OHM

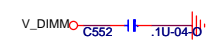
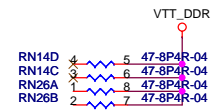
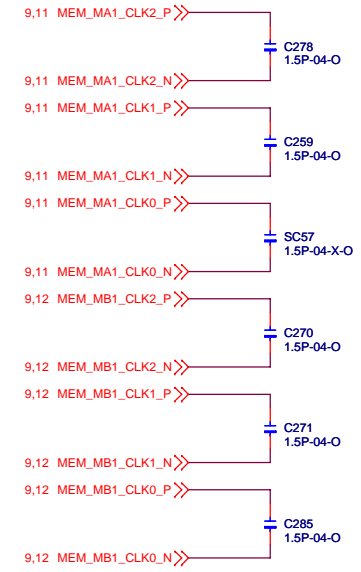
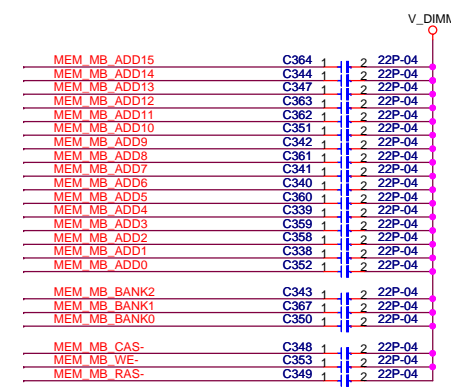
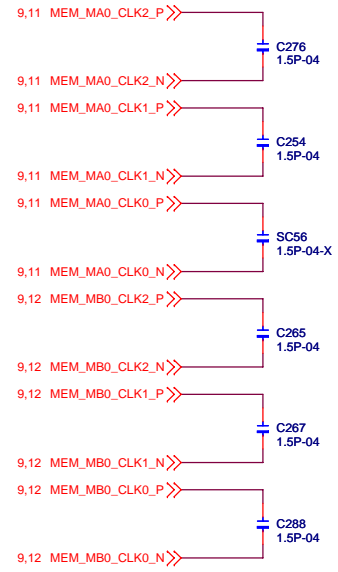
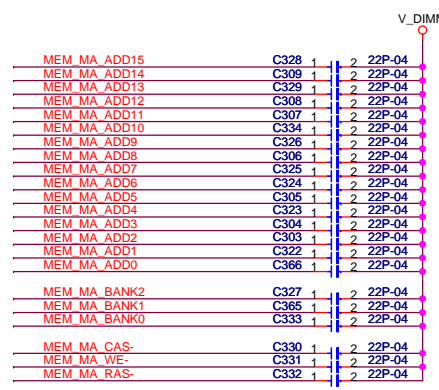
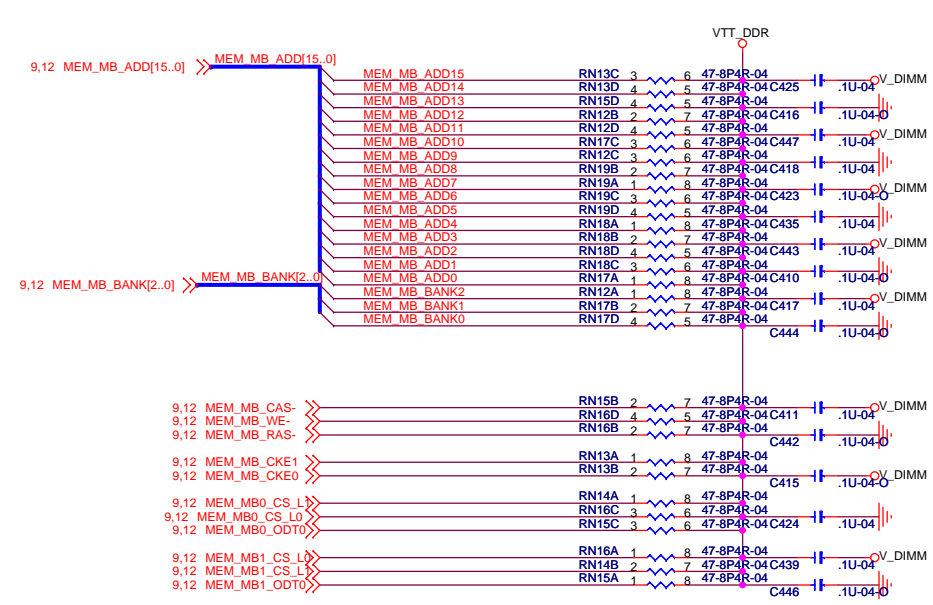
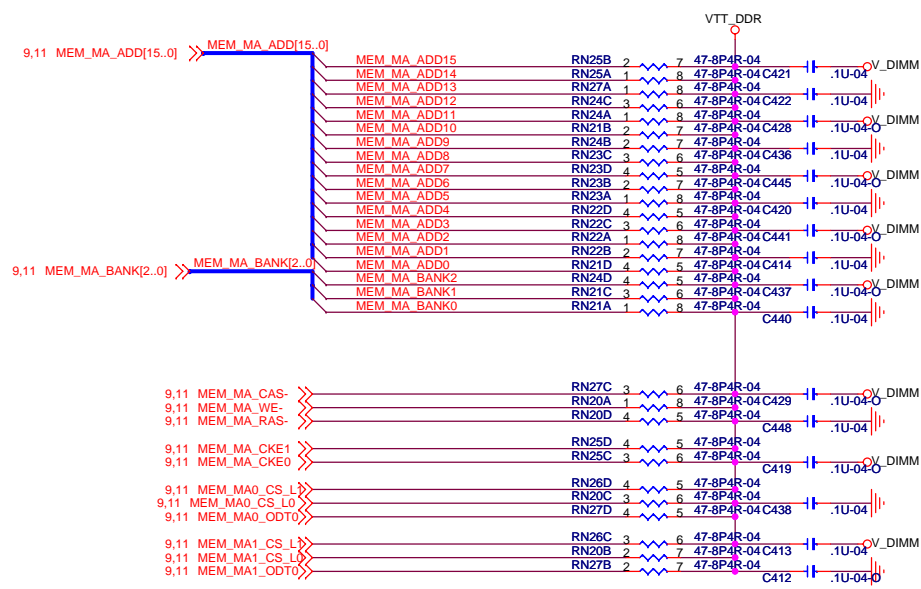
AMD USE 59 OHM

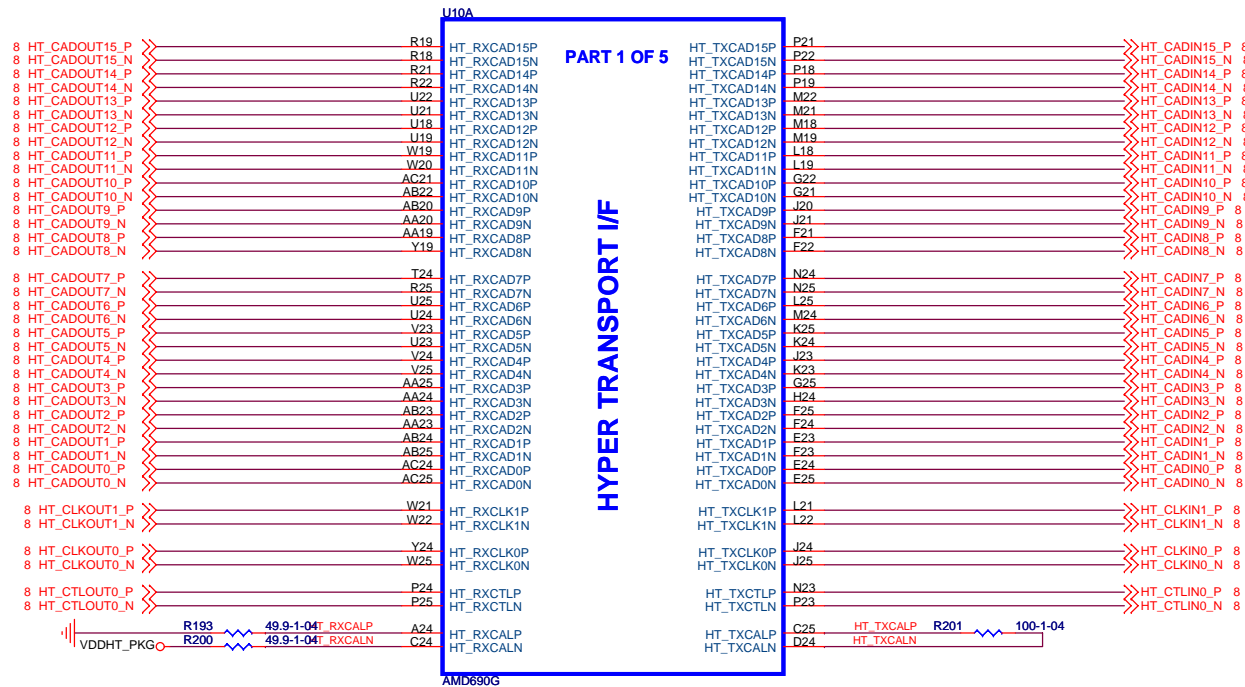






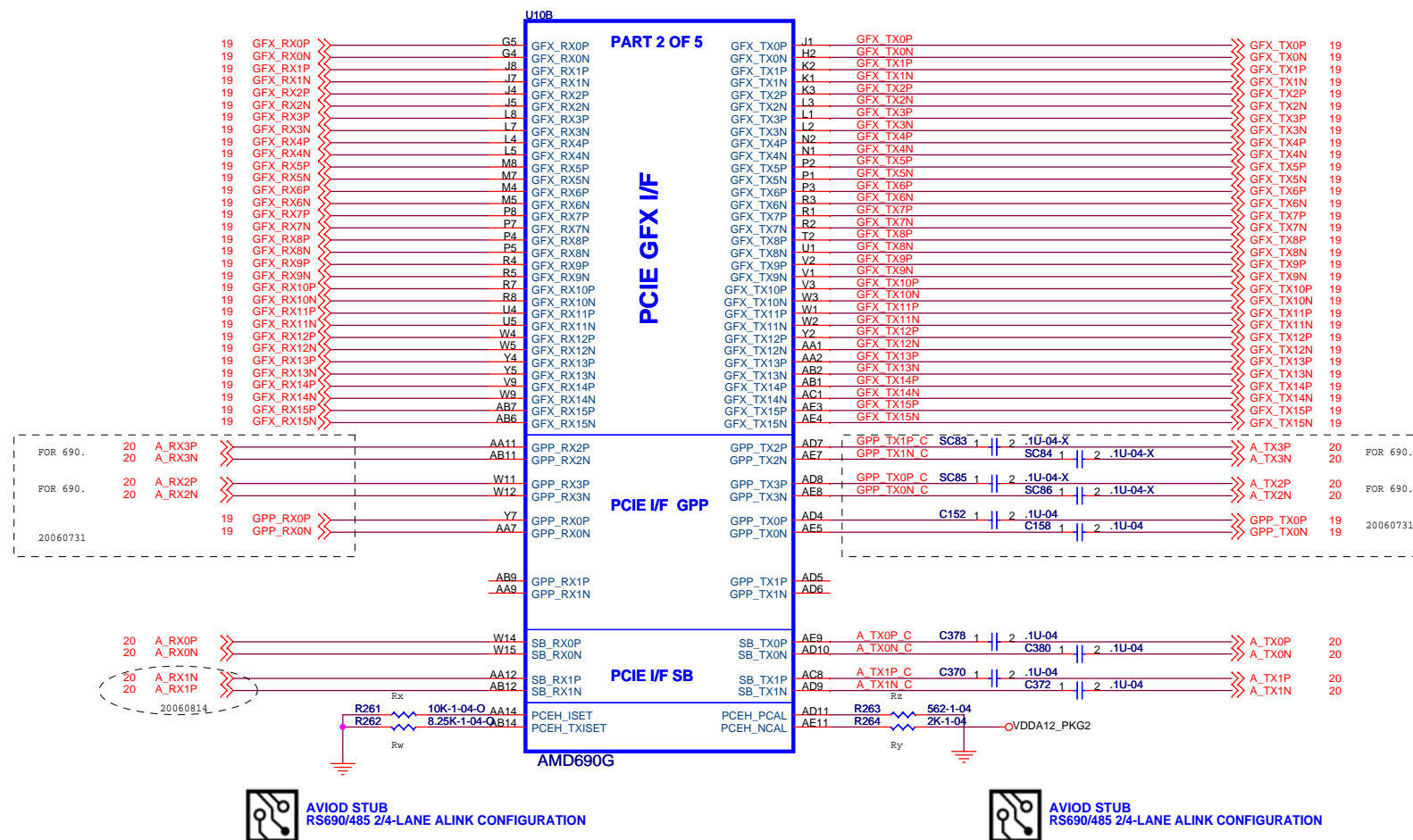






VCC1.2 C544 1 2 .1U-04-O VCCORE

VCC3 C545 1 2 .1U-04-O VCCORE

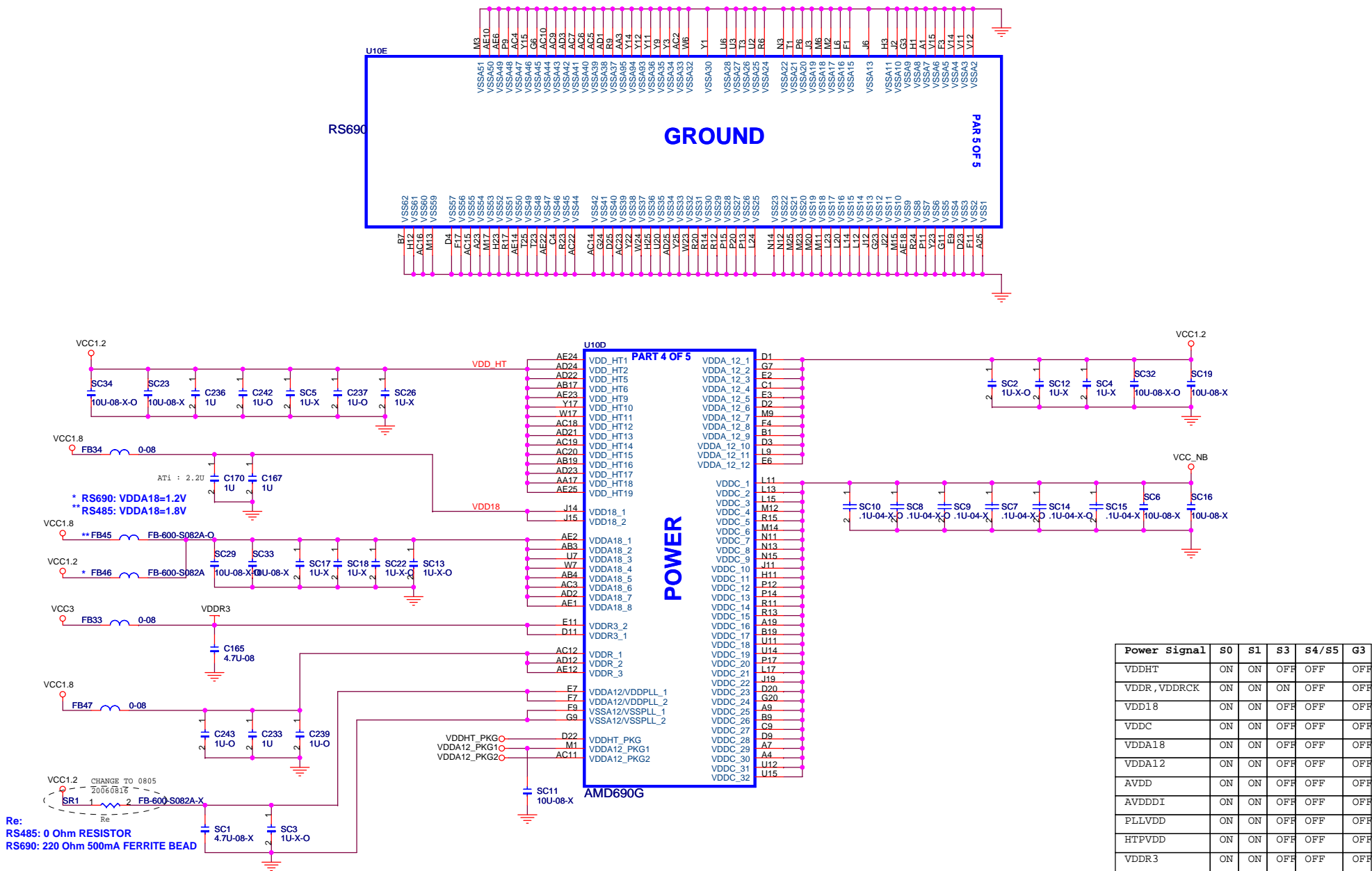


**RS690/RS485 CHANGE TABLE**

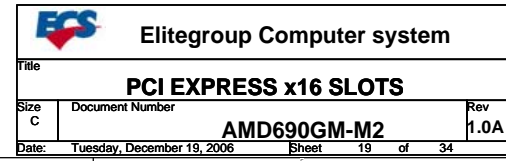
NB/DIFF	Rw	Rx	Ry	Rz
RS690	DNI	DNI	2K	562R
RS485	8.25K	10K	82.5R	150R







+12V: 5.5Amp



SB CALIBRATION RESISITOR VALUE	
	SB600
Ra	562 OHM 1%
Rb	2.05K 1%
Rc	0

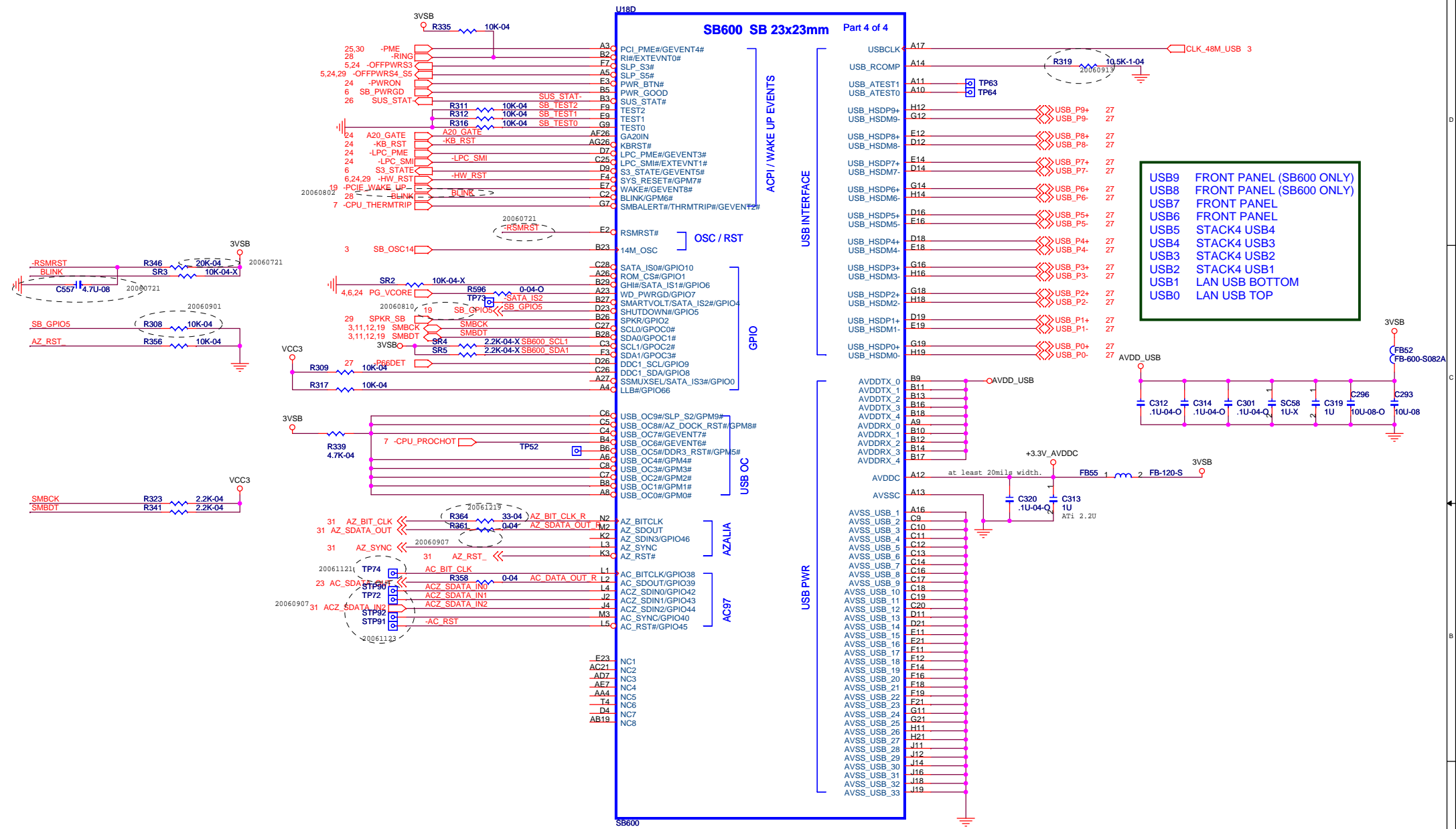
FOR SB600 VCC\_SB= 1.2V

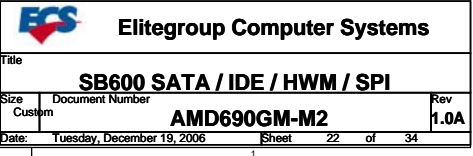
PLACE THESE COMPONENTS CLOSE TO U600, AND  
USE GROUND GUARD FOR 32K\_X1 AND 32K\_X2

LPC PULL UPS

FOR SB600, THIS BALL IS LDRQ1 ONLY

1-2: NORMAL  
2-3: CMOS CLEAR

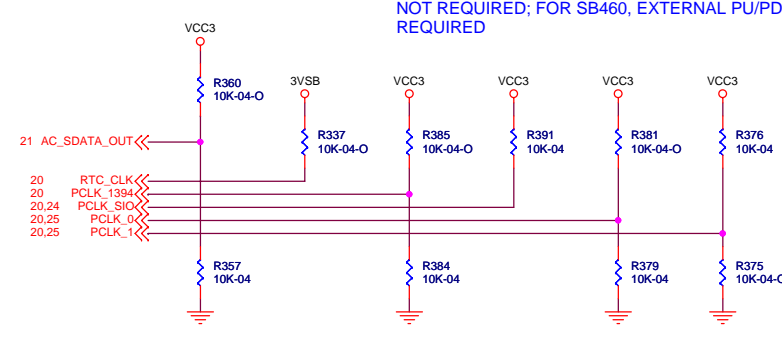




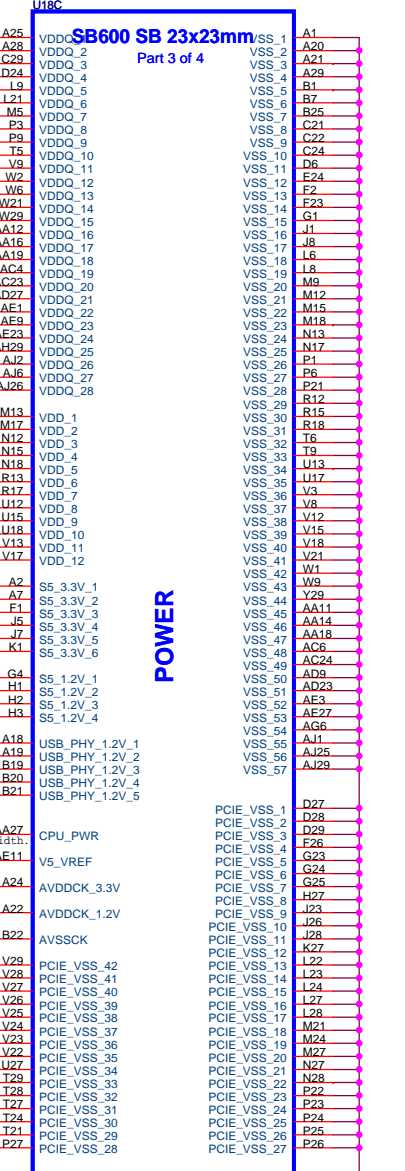
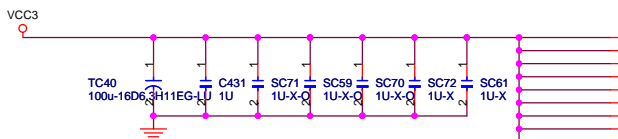


REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC\_SDATA\_OUT,  
15K PU FOR RTC\_CLK, EXTERNAL PU/PD IS  
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE  
REQUIRED



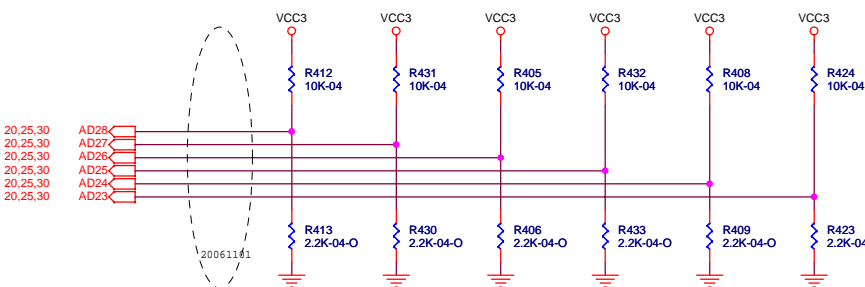
		SB600		SB460	
		AC_SDOUT	RTC_CLK	PCI_CLK4 (PCLK_1394)	PCI_CLK6 (PCLK_SIO)
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC II ROM L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	ROM TYPE: H, H = PCI ROM H, L = LPC II ROM L, H = LPC II ROM L, L = FWH ROM
		DEFAULT	DEFAULT	DEFAULT	NOTE: FOR SB460, PCLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCLK[1:0]



POWER

DEBUG STRAPS

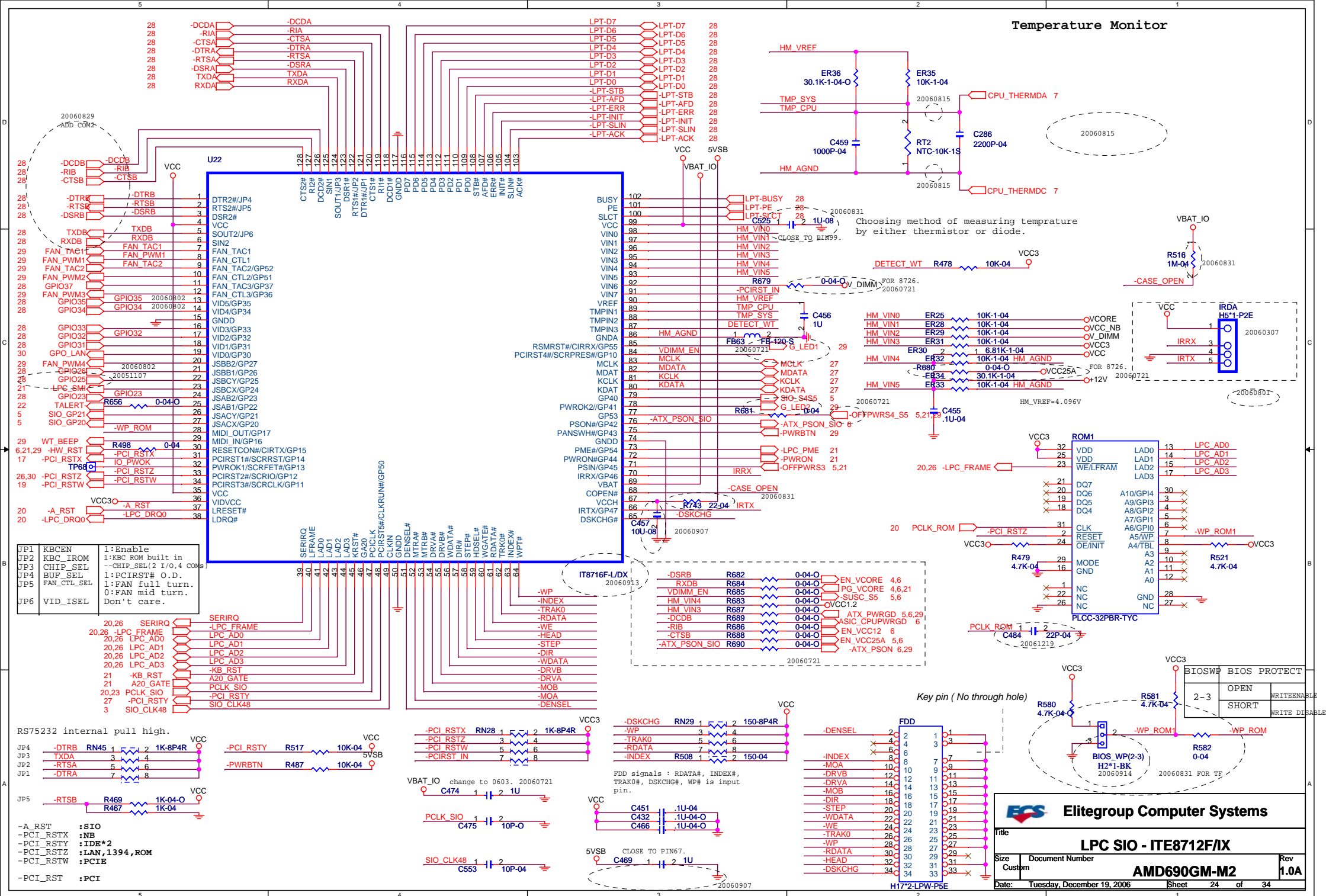
SB600 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



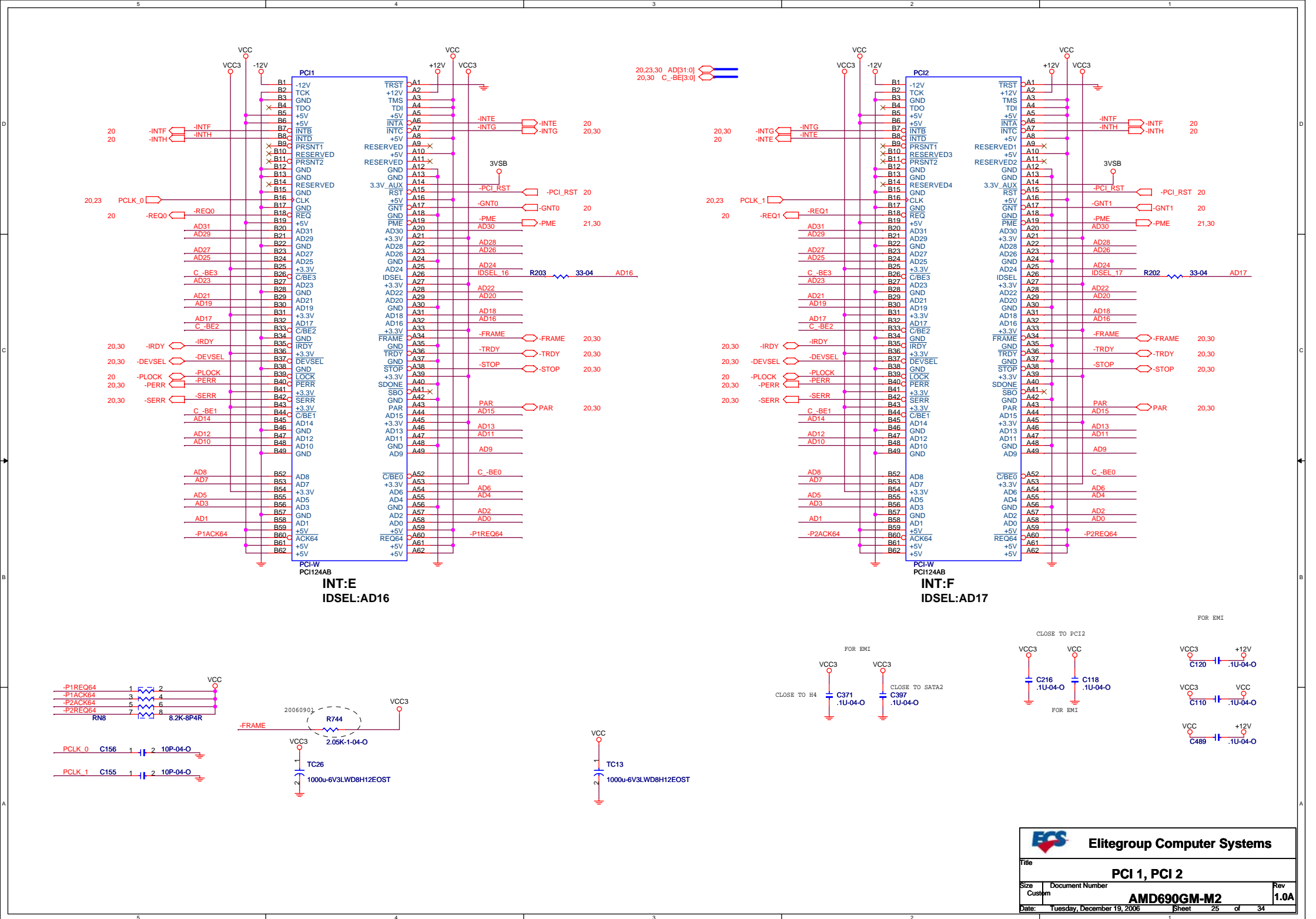
2.2K IF USED FOR SB600.  
10K IF USED FOR SB460.

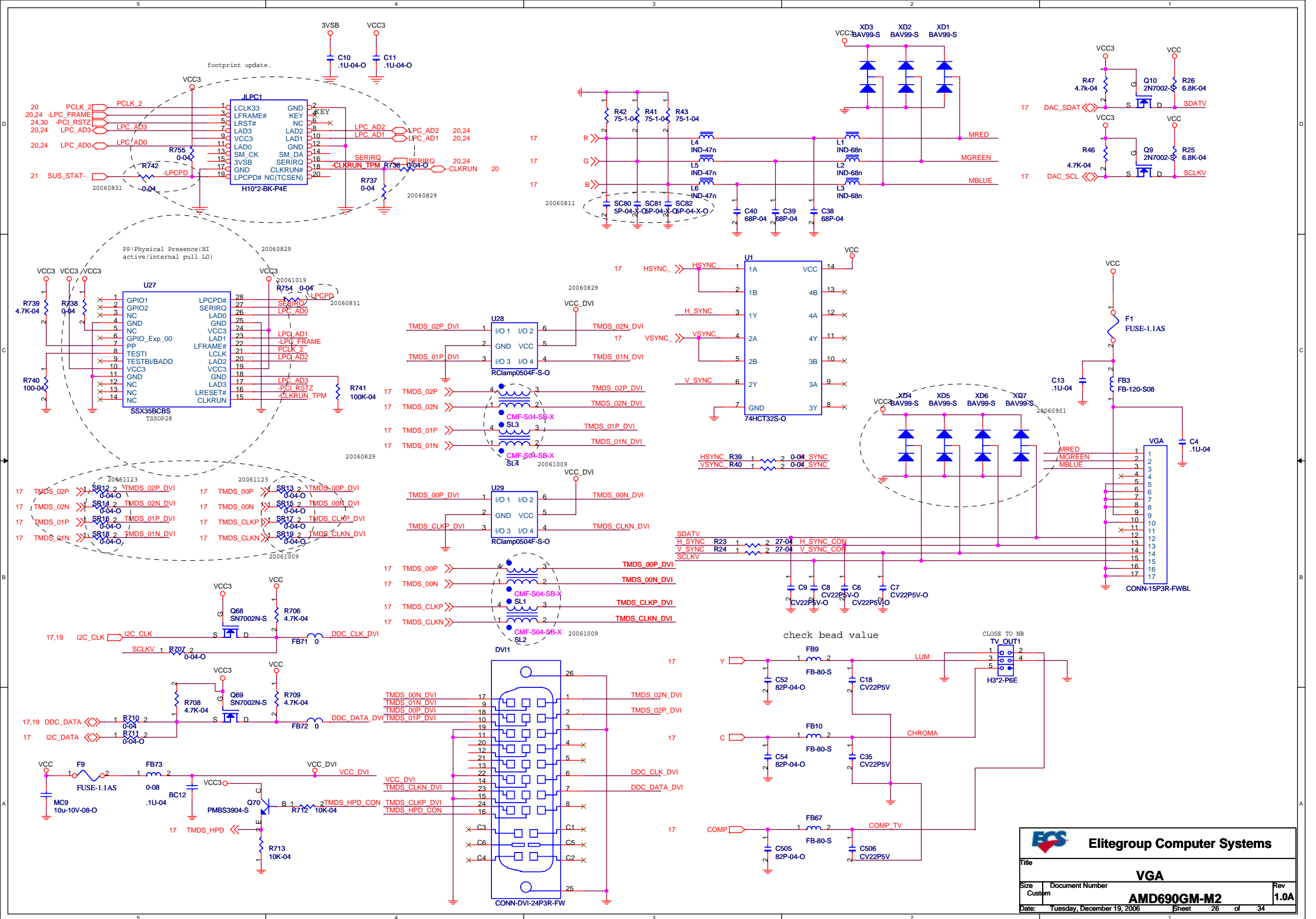
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED
		DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT

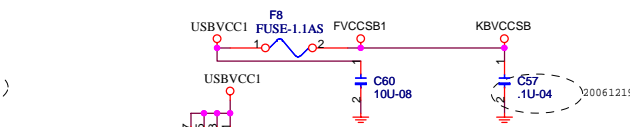
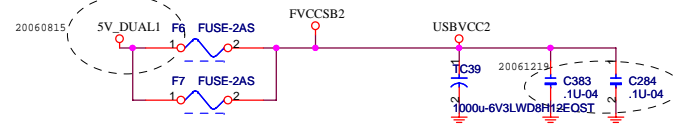
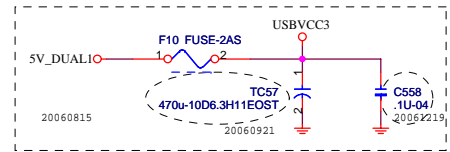
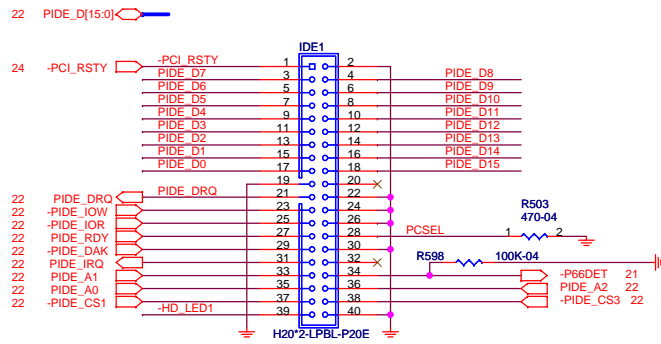
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



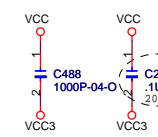
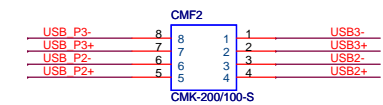
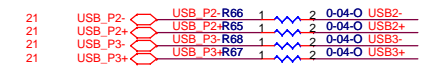
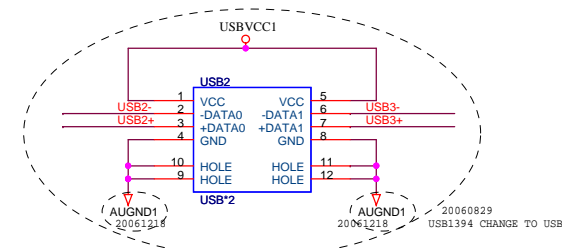
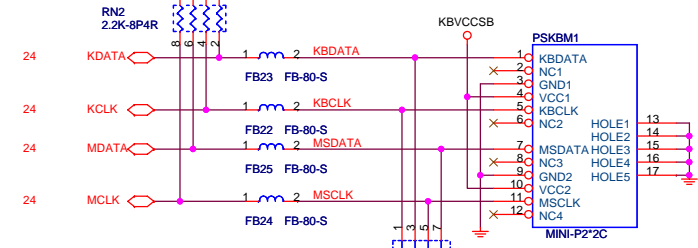
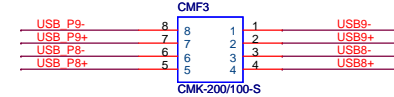
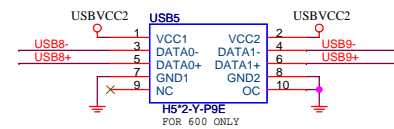
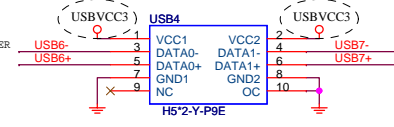
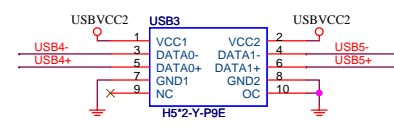
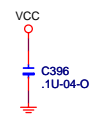
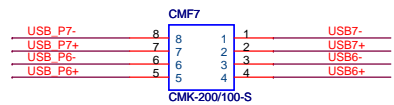
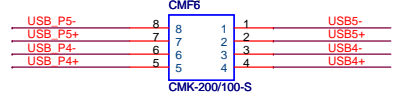
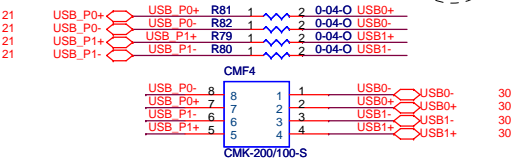
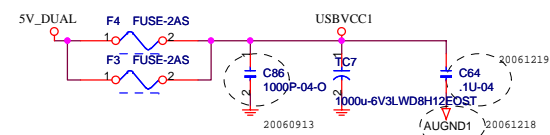








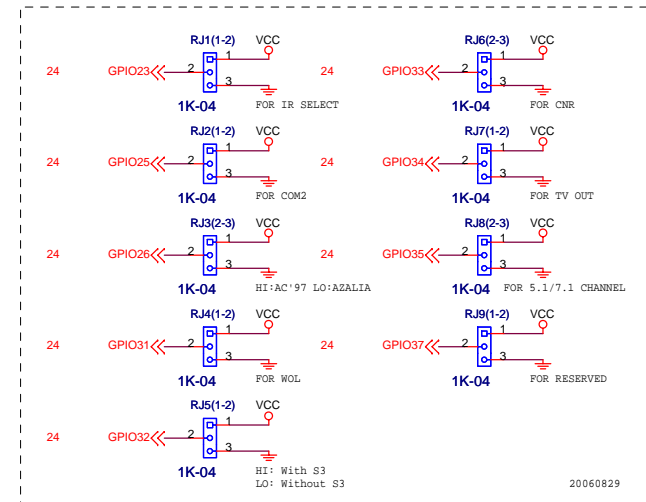
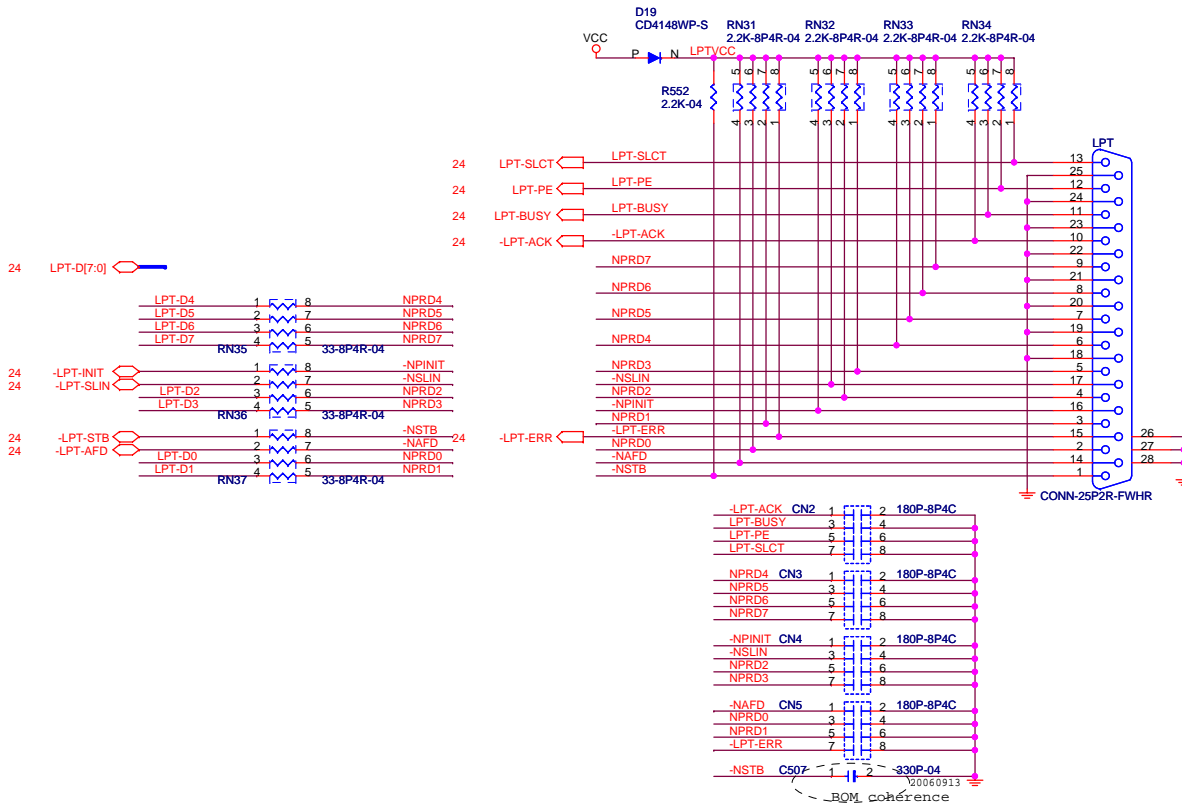
## USB 0-1



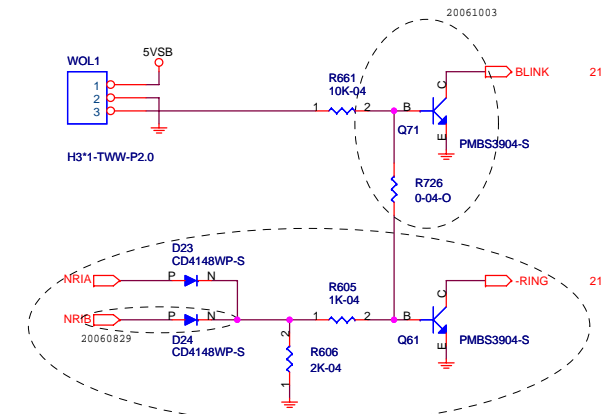
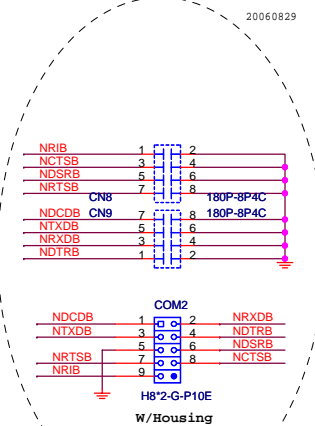
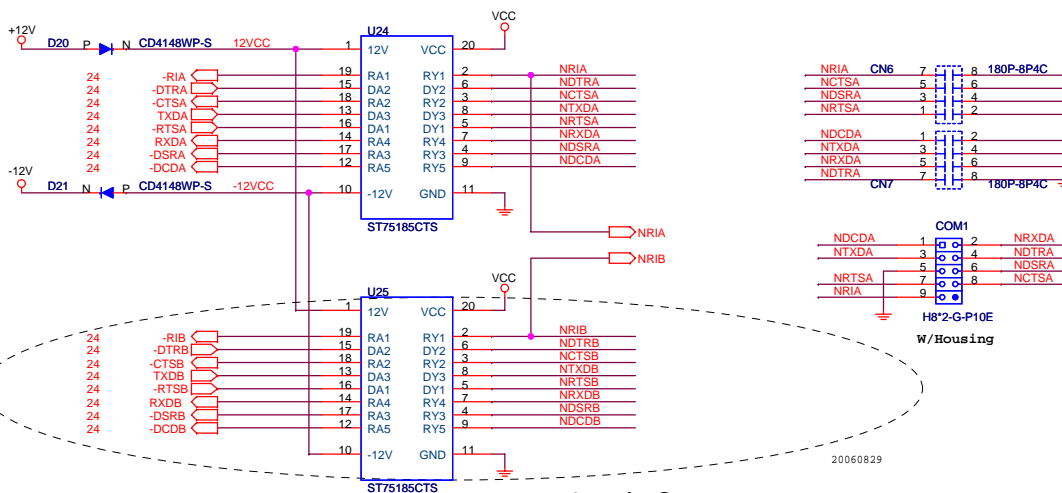
**Elitegroup Computer Systems**

Title			USB, IDE
Size	Document Number	Rev	
Custom		1.0A	
Date:	Tuesday, December 19, 2006	Sheet	27 of 34

**LPT**



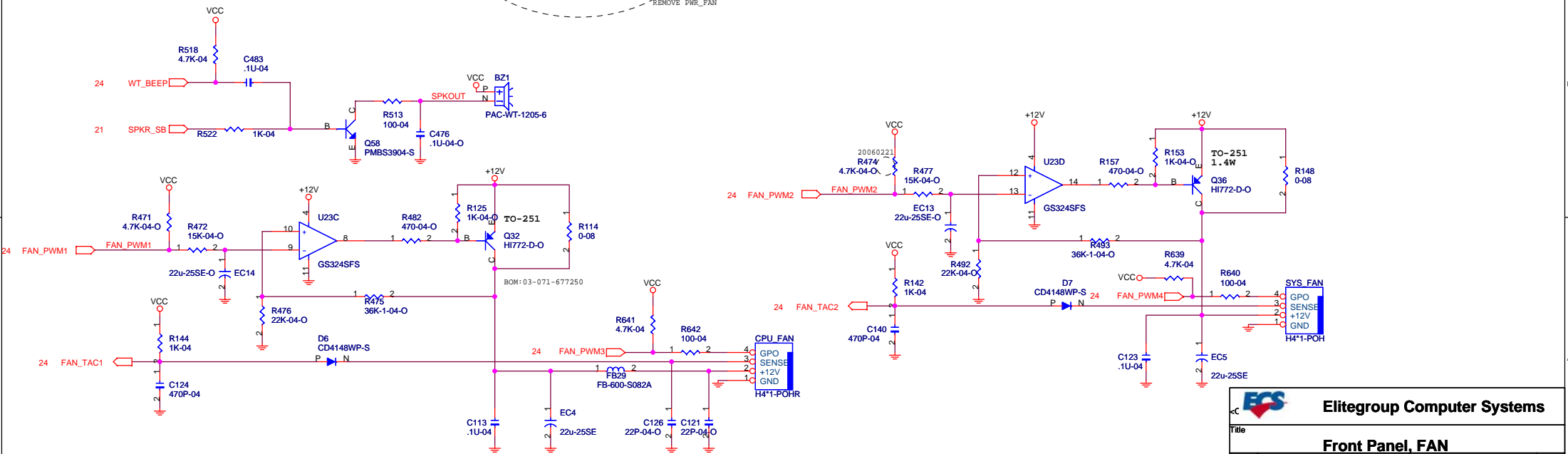
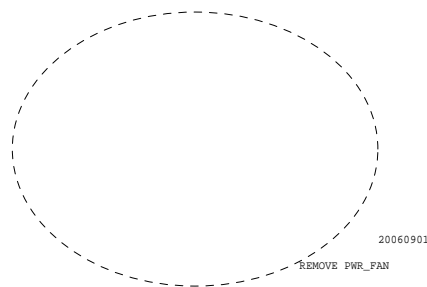
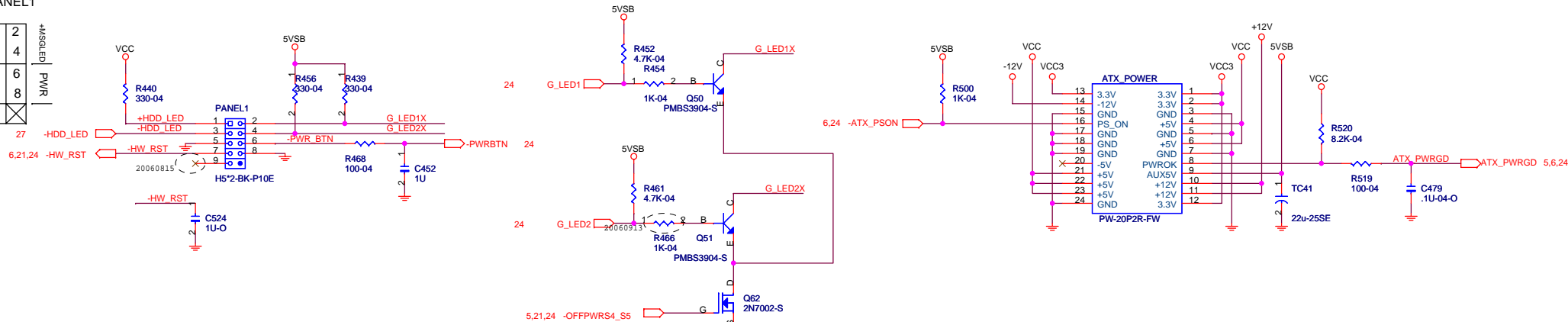
**COM 1**

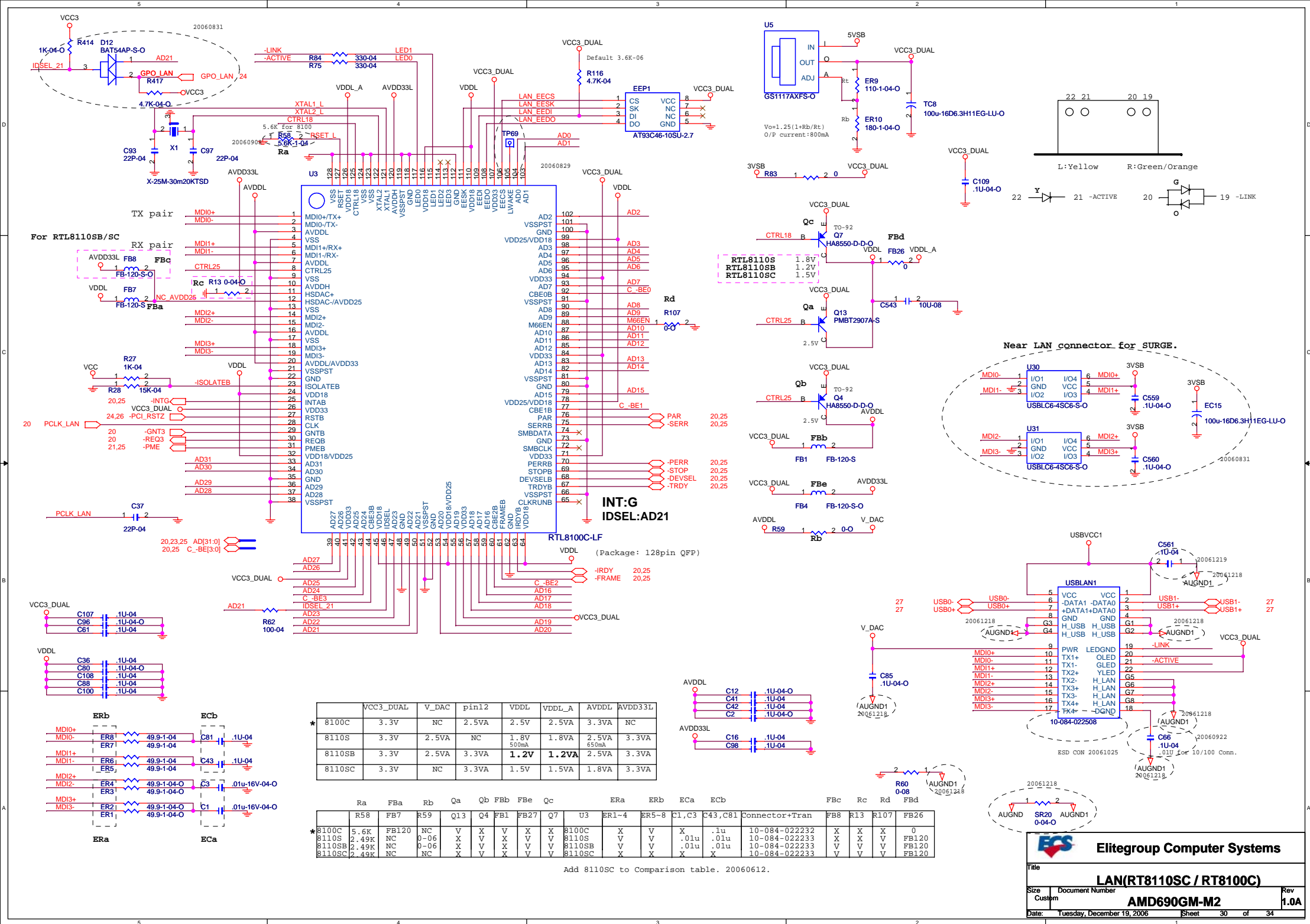


**COM 2**

# PANEL1

1	2	+HDD_LED
3	4	
5	6	+HDD_LED
7	8	
9	9	RST

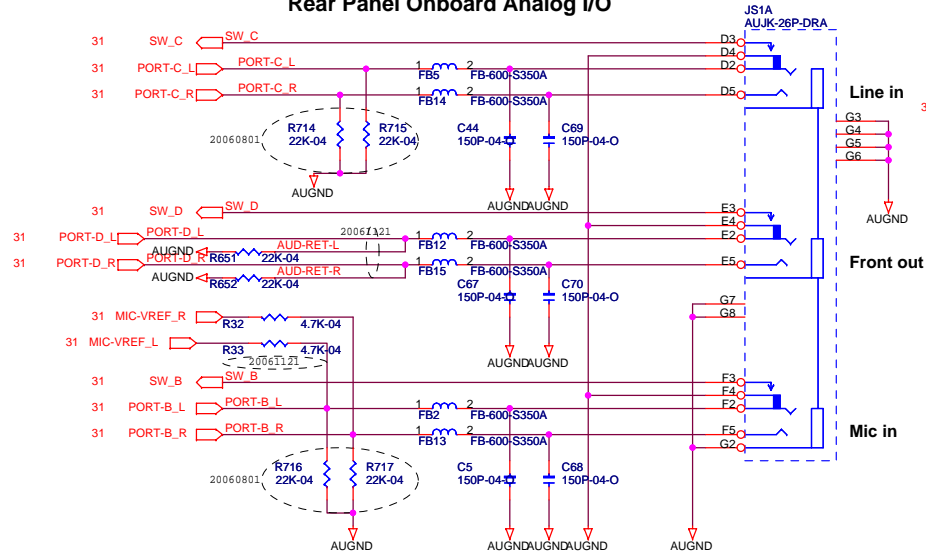




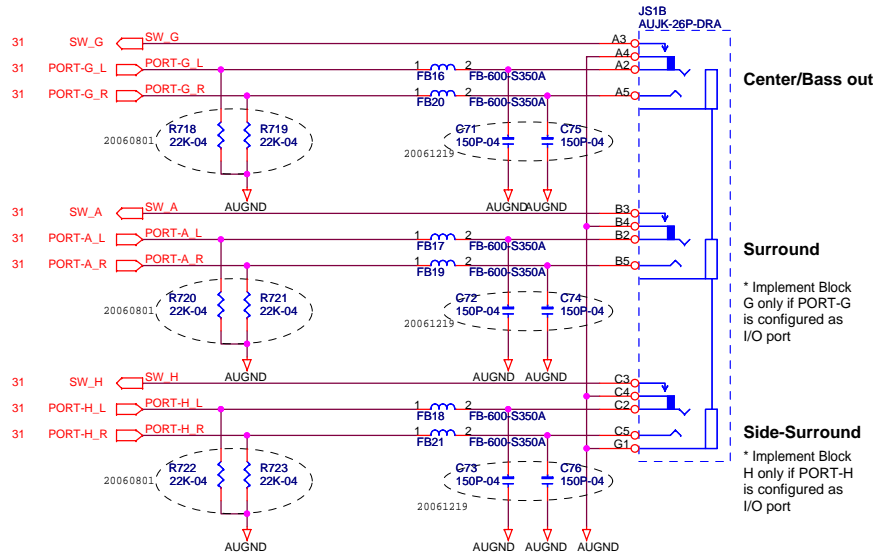




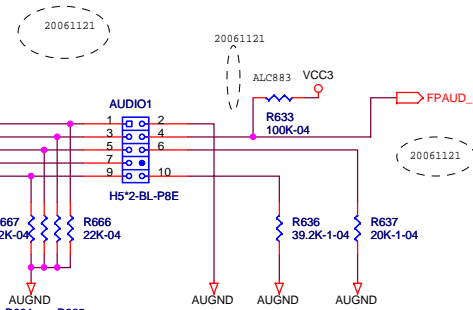
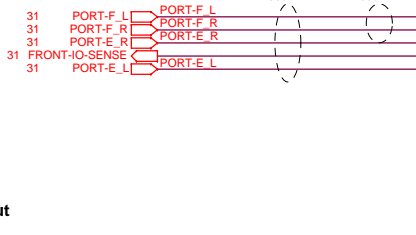
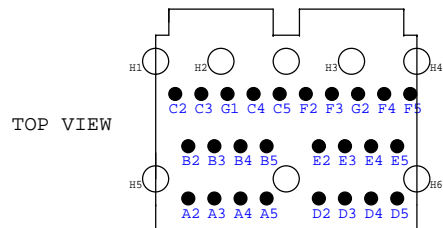
## Rear Panel Onboard Analog I/O



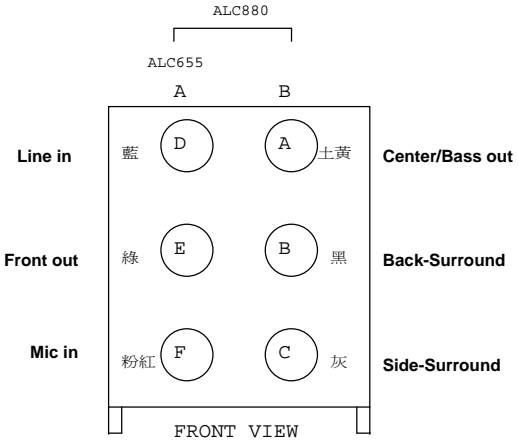
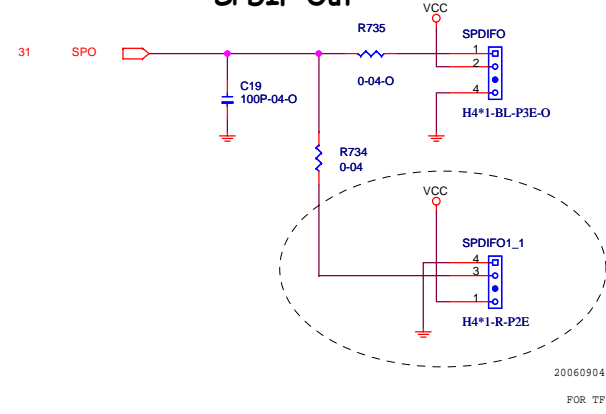
## Rear Panel (Optional Rear Audio Panel)



The schematic should consist with PINs define of I/O connector.



## SPDIF Out





ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

CPU PW
12V +/-5%

VRM SW  
REGULATOR

VDD\_CPUCORE\_RUN (S0, S1)

1.2V LINEAR  
REGULATOR

VDDHT\_1V2 (S0, S1)

VCC 1.2V SW  
REGULATOR

VDDA\_1V2 (S0, S1)

2.5V LINEAR  
REGULATOR

AVDD(S0, S1)

1.8V SW  
REGULATOR

+1.8V(S0, S1)

2.5V SHUNT  
REGULATOR

VDDA\_2.5\_RUN  
(S0, S1)

2.5V SHUNT  
REGULATOR

VDD\_2.5\_RUN  
(S0, S1)

DUAL REGULATOR

1.8V VDD SW  
REGULATOR

0.9V VTT\_DDR  
REGULATOR

VTT\_DDR\_SUS (S0,S1,S3)

+3.3VSB REGULATOR  
ACPI CONTROLLER

+3.3VSB (S0, S1, S3, S4, S5)

+3.3V\_DUAL (S0, S1, S3, S4, S5)

+5V\_DUAL (S0, S1, S3, S4, S5)

+5V\_DUAL1 (S0, S1, S3, S4, S5)

+5VDUAL\_MEM (S0, S1, S3, S4, S5)

1.8V STB LDO  
REGULATOR

+1.8VSB (S0, S1, S3, S4, S5)

+3.3V (S0, S1)

5VAA LDO  
REGULATOR

+5VAA (S0, S1,S3)

GBE	
3.3V 0.5A (S0, S1)	
3.3V 0.1A (S3)	

SATA	
3.3V 0.3A (S0, S1)	

AC97/AZALIA	
3.3V CORE 0.3A	
5V ANALOG 0.1A	

SUPER I/O	
+5V SD 0.01A	
+5V 0.1A	

SB600	
X4 PCI-E 0.8A	
ATA I/O 0.2A	
ATA PLL 0.01A	
PCI-E PVDD 80mA	
SB CORE 0.6A	
1.8V S5 PW 0.22A	
3.3V S5 PW 0.01A	
USB CORE I/O 0.2A	
3.3V I/O 0.45A	

RS485/RS690	
VDDHT 1.2V 0.5A	
PCI-E CORE &VCO 2.25A	
NB CORE VDDC 1.0-1.2V 5A	
DAC 200mA LVDS 1.8V 300mA	
PLL & DAC-Q 0.1A	
PCI-E I/O 1500mA	

M2	
VDDA 2.5V 0.1A	
VDDCORE 0.8-1.55V 80A	
DDRII MEM I/F VTT 0.125A, VDD 3A	
VLDI 1.2V 0.5A	

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIE	
3.3V	3.0A
12V	5.5A


CNR CONNECTOR	
5V	1.0A
3.3V	1.0A
12V	0.5A
3.3Vaux	1.0A
-12V	0.1A
5VDual	0.5A

USB X4 FR	
VDD	
5VDual	2.0A

USB X6 RL	
VDD	
5VDual	2.0A

2XPS/2	
5VDual	1.0A

+3.3VDUAL (S0, S1, S3)

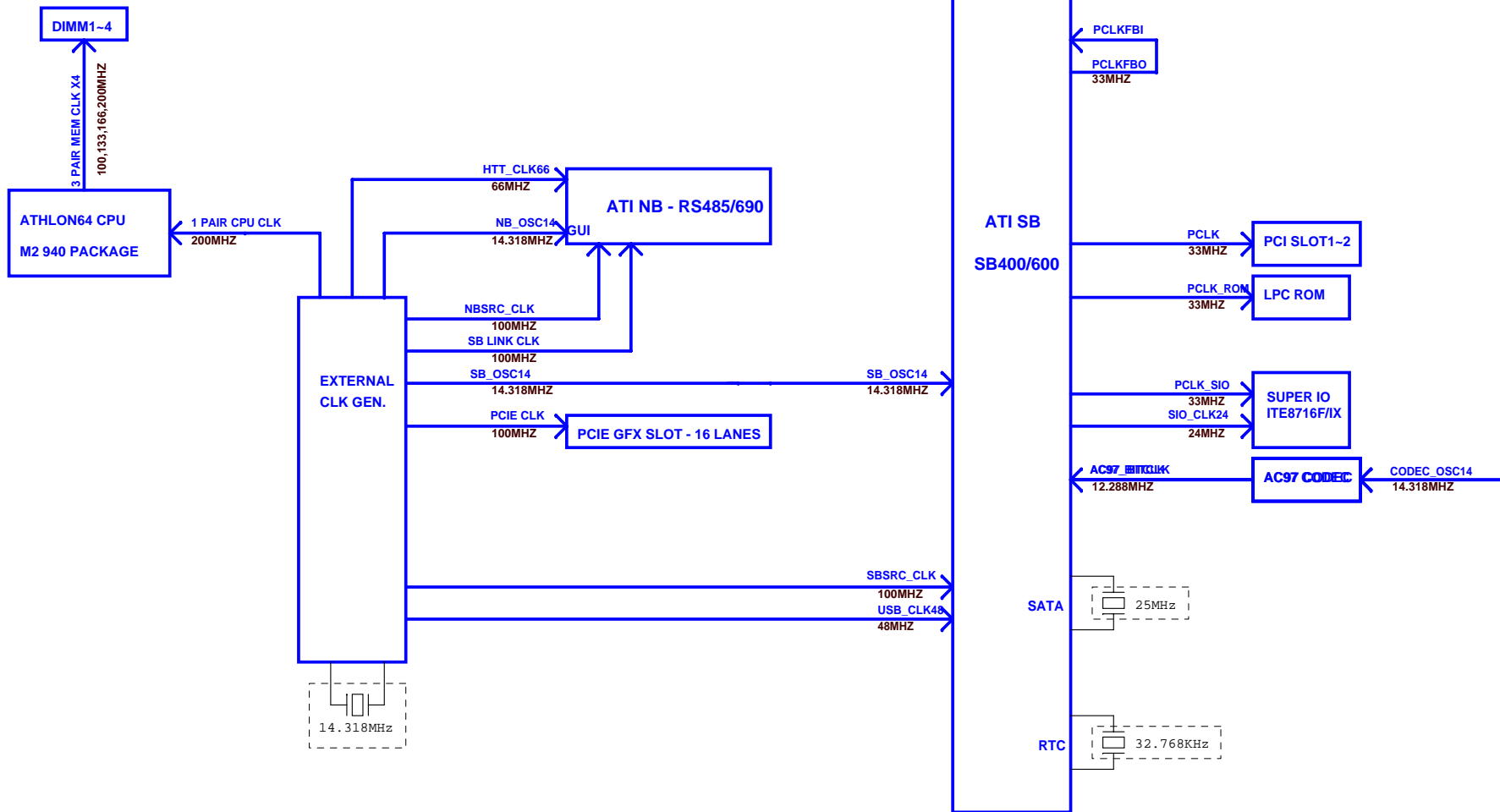

**Elitegroup Computer Systems**

Title

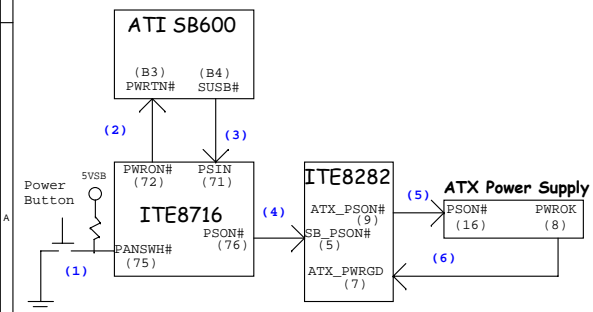
**POWER DELIVERY CHART**

Size Custom Document Number **AMD690GM-M2** Rev **1.0A**

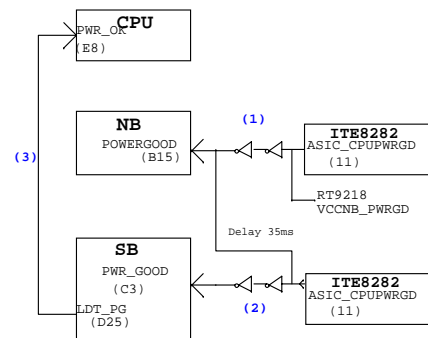
Date: Monday, December 18, 2006 Sheet 33 of 34



### Power On



### Power Good



### Reset Tree

